Research Article

Bridgeless SEPIC Power Factor Correction Rectifier in DCM with reduced losses

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Abstract: Single phase AC-DC bridgeless SEPIC power factor correction (PFC) rectifier in discontinuous conduction mode is proposed. In this topology conduction losses are less with improved thermal management. During each switching cycle two semiconductor switches are only present in current flowing path. In a effective simple manner unity power factor is achieved through discontinuous conduction mode. Control circuit complexity is reduced by soft switching of power switches and zero current turn off of output diode. Conventional SEPIC PFC rectifier is compared with the proposed topology. PI controller compensates the error and maintains unity power factor. The results obtained from simulation and experiment show the effectiveness of the proposed topology.

Keywords: Bridgeless power factor correction (PFC) rectifier, discontinuous conduction mode (DCM), proportional integral(PI) controller, SEPIC.

1.Introduction

In industries power factor correction is important issue due to industrial load causing current delay and harmonics of higher order. It is necessary to charge the industrial customers for reactive power consumption. Active PFC circuits are commercially used for power factor correction. Unity load power factor is achieved by making load behave like resistor. Input line current harmonics is low. Active PFC and SMPS available in market consist of bridge rectifier and dc-dc converter operating at high frequency. Fig. 1 shows a conventional SEPIC PFC rectifier.

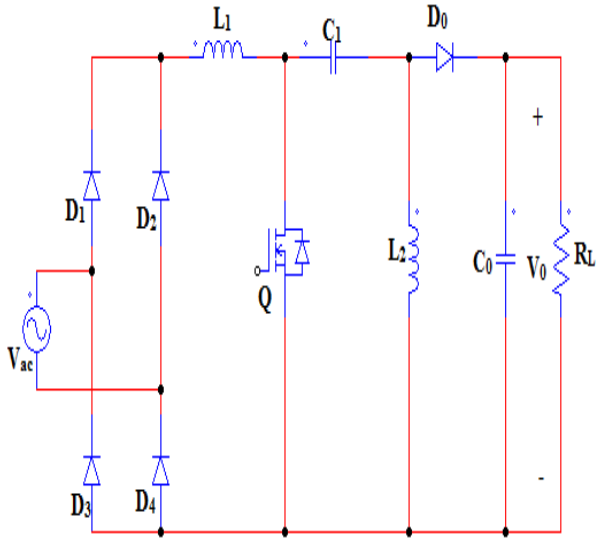

Fig.1 Conventional SEPIC PFC rectifier topology

Current flows through three semiconductor devices during each switching cycle . This is suitable for low power application. In case of low line input and high power applications efficiency gets reduced due to voltage drop in bridge rectifier and high conduction losses. It is necessary to use diode with high current handling and good heat dissipation capability which increases the size and cost of the circuit. So it becomes necessary to develop efficient bridgeless PFC circuits. In such circuits current flows through less semiconductor devices which lowers conduction and switching losses thereby improving efficiency. . Efforts are taken to develop efficient bridgeless power factor correction circuit topologies for low line input and high power applications [1]-[2]. In bridgeless PFC during each switching cycle current flows through two semiconductor device which reduces conduction losses and heat generation thereby improving efficiency. Cost gets reduced due to less semiconductor devices. Bridgeless topology makes use of boost converter because of its simplicity, efficiency, low cost and high performance. In [3] a boost rectifier operating with ZVS PWM is developed. Soft commutation of all semiconductor devices including main switch reduces voltage and current stress. This increase efficiency and improves power factor but additional auxiliary circuit for zero voltage switching and hall effect sensor for sensing the input current signal is required. Continuous conduction boost converters are simple and capable of handling high power. So this is used for PFC circuits. But high output voltage and current leads to severe reverse recovery problem. A bridgeless boost rectifier with reduced diode reverse recovery problem for PFC is proposed in [4] . A coupled inductor and two diode in the circuit alleviates the problem of reverse recovery of diode and reduced conduction losses but makes use of large filters and current transformer to sense the switching current which is a drawback. In [5] single stage symmetrical half bridge high power factor electronic ballast for fluorescent lamps is developed. This consists of a boost PFC with half bridge inverter. The conduction losses are reduced in this topology. Two approach to minimize common mode noise emission in bridgeless PFC converters is discussed in [6]. In first approach symmetry is achieved by modifying bridgeless PFC. In second approach a balance technique is introduced to minimize common mode noise. For CCM and DCM bridgeless PFC boost rectifier performance evaluation is done in [7].The drawbacks of boost PFC circuit are DC output voltage are higher than peak input voltage, no isolation between input and output voltage, high start up inrush current ,no current limiting during overload condition. Active PFC current and SMPS in market are looking for bridgeless PFC circuit topology. Advantages of boost converter in DCM are simple control PFC circuit, main switch soft turn on and reduced reverse recovery loss of diode. Boost inductor of high quality is required to switch high peak ripple current and voltage in DCM operation. In [8] and [9] two bridgeless topologies are proposed. This is suitable for step up/step down applications. In [8] three semiconductor switches is present in current conduction path during each switching period. This requires an isolated gate drive. The topology in [9] has one or two semiconductor in current conduction path with reduced voltage stress across semiconductor device but requires isolated gate drive. In this circuit high frequency component of pulsating input current is suppressed by employing a robust input filter. This increases the cost and weight of the inductor. In [10] single phase SEPIC PFC converter GA tuned PI controller is proposed for variation in line, load. In [11] bridgeless buck PFC operating in DCM with simple controller is proposed to reduce the dead angle of input current and improve power factor. In [12]modified multiplier SEPIC PFC with PI and PID controller is compared with conventional single stage SEPIC PFC.

In this work bridgeless SEPIC PFC circuit in DCM mode is proposed. The advantage of this circuit is less inrush current while starting and overload condition, low ripple in input current, less electromagnetic interference, easy implementation of transformer isolation.

2. Bridgeless SEPIC PFC circuit working

Topology of single-phase ac–dc bridgeless SEPIC power factor correction rectifier is shown in Fig.2. In this circuit during each switching cycle only two semiconductor switch is present in current flowing path which reduces the conduction loss. Absence of input diode bridge improves thermal management. Unity power factor is achieved in a simple and effective manner by making the circuit work in discontinuous conduction mode (DCM). Power switch zero-current turn-on and output diode zero-current turn-off helps in reducing the complexity of the control circuit.. The PI controller controls output to input relation. The error between actual and reference voltage is minimized by PI controller. Line side power factor is maintained for all loads.

Table. 1. Comparison of bridgeless and conventional SEPIC PFC rectifiers

Item		**Conventional SEPIC PFC**	**Bridgeless SEPIC PFC**
Switch		1	2
slow diode		4	2
fast diode		1	1
current conduction path	stage 1	2 slow diode,1switch	1 slow diode,1switch
	stage 2	2slow diode,1fast switch	1 slow diode,1fast switch
	DCM	1 slow diode	1 slow diode

In this proposed topology two DC SEPIC converters are connected. One operates during each half line period of input current. Two semiconductor devices are present in the current flowing path which reduces conduction loss of the circuit. The switches Q_1,Q_2 input inductor L_1, L_2 and coupling capacitor C_1 ,C_2 are subjected to lower RMS current stress compared to conventional SEPIC. The thermal stress on the semiconductor device gets reduced and the efficiency of the circuit increases compared with conventional SEPIC rectifier. The slow recovery diode D_P and D_N connect the input line AC voltage to ground and reduces the noise due to common mode EMI. Present topology has three inductors compared to two in conventional SEPIC. In input current zero ripple can be achieved for DCM operation which reduces the noise due to EMI and it also reduces input filtering requirements. The current stress is less in switch compared to conventional SEPIC rectifier because each switch operates for only half cycle. The voltage stress is equal in both proposed circuit as well as conventional SEPIC. The bridgeless rectifier proposed has two DC-DC SEPIC convertors. During positive half cycle diode D_P, L_1,Q_1, L_3, D_0 is active .In negative half cycle L_2,Q_2,C_2 ,L_3,D_0 is active with diode D_N. This is a symmetric circuit with inductors operating in DCM. Due to symmetry of circuit it is enough to analyse positive half cycle of the circuit. The advantage of operating the rectifiers in DCM is near unity power factor turn on of power switch at zero current, turn off of output diode D_0 at zero current which result in low switching loss, reduced output diode reverse recovery voltage.

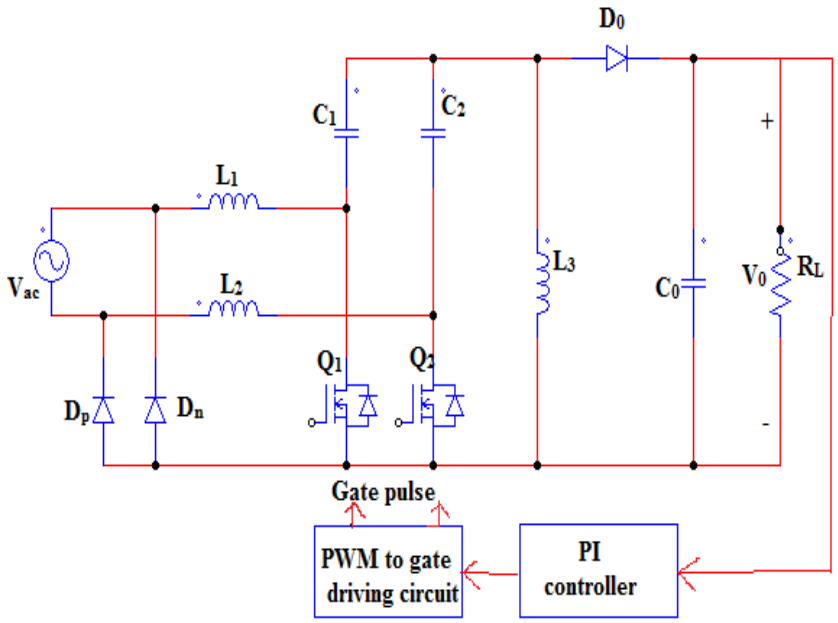

Fig. 2. Bridgeless SEPIC PFC Circuit

2.1 Operating Principle

There are three operating modes in positive half switching period T_s.

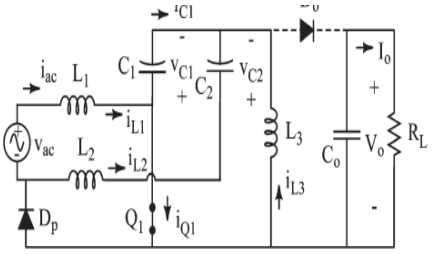

Fig.3 Switch On duration

Stage 1

Fig.3 shows switch on period. During switch Q_1 on current i_{L1} and i_{L2} from inductor will forward bias D_p, input voltage will reverse bias D_N. V_{ac} and V_0 will reverse bias output diode D_0. Current in inductor $i_{L1,}$ $i_{L2,}$ i_{L3} increases proportional to input voltage *v*ac. Switch current during this time will be sum of three inductor currents. At the end of this stage the switch is turned off.

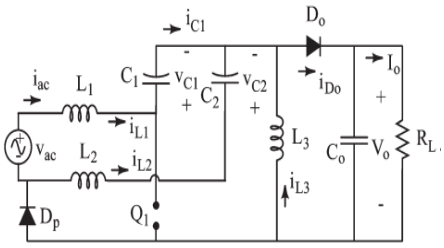

Fig.4 Switch Off duration

Stage 2

Fig.4 shows switch off period. Switch Q_1 is off. D_o diode gets on and provides a path for the three inductor currents. D_p conducts and provides a path for i_{L1} and i_{L2}. All inductor currents decreases linearly proportional to the output voltage V_o. At the end of this interval current i_{Do} reaches zero. Diode D_o becomes reverse biased.

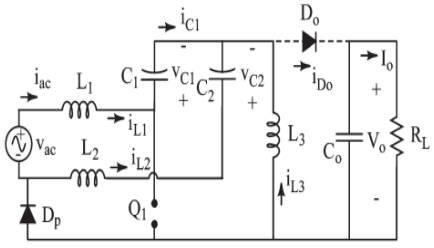

Fig.5 DCM condition

Stage 3 (t_2,T_s)

Fig.5 shows DCM condition. Q_1 and D_o are in off-state. i_{L3} flows through diode D_p. The current is kept constant by the three inductors which act as current sources. The voltage across the three inductors is zero. During this mode i_{L1} charges C_1 and C_2 is discharged by i_{L2}.

The same control circuit can drive both the switches. The circuit complexity and cost is reduced.

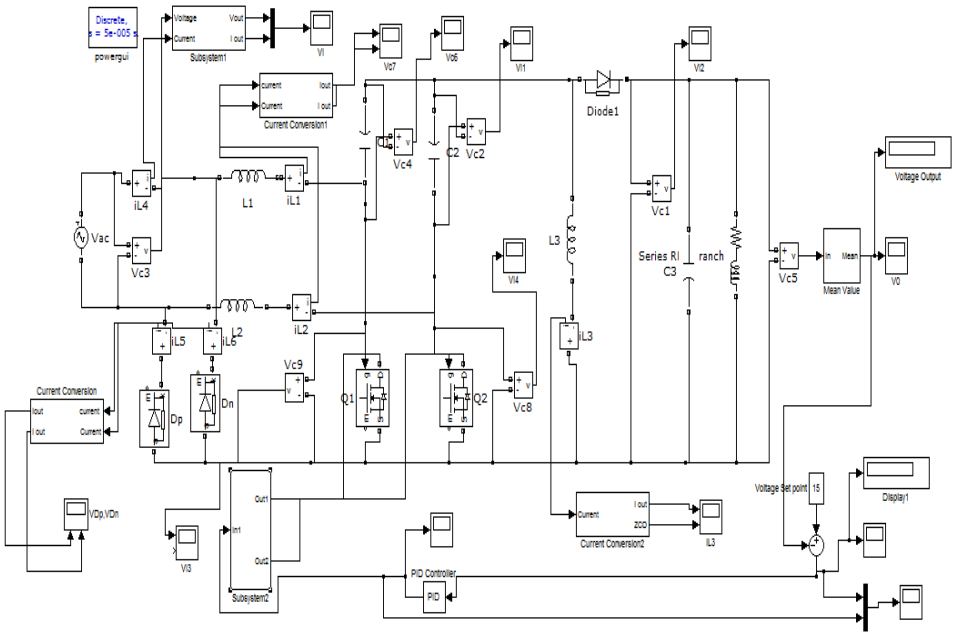

Fig 6. Simulation circuit of Bridgeless SEPIC

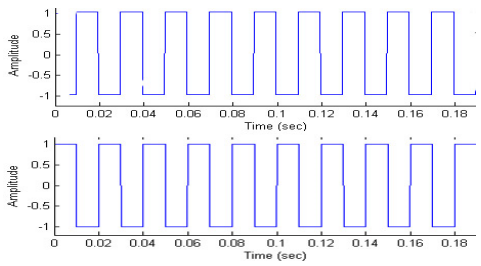

Fig. 7. Gating Signal

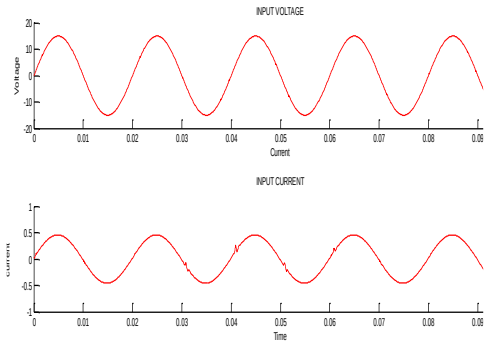

Fig.8. Input voltage and current

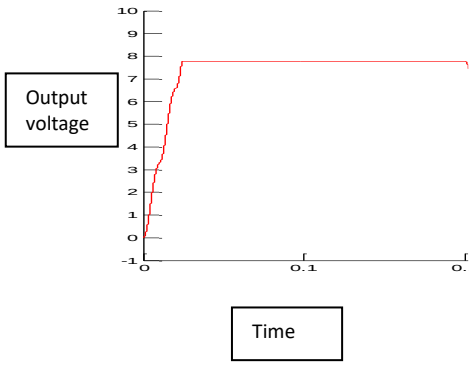

Fig.9. Simulated output Voltage

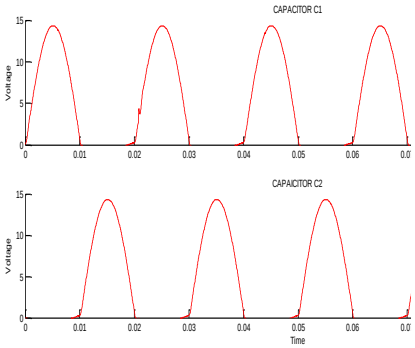

Fig.10. Capacitor Voltage during simulation

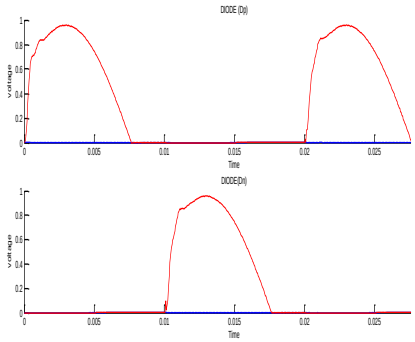

Fig.11.Voltage across doide during simulation

Fig.6 shows simulation circuit of bridgeless SEPIC. Fig.7 shows the gate pulse applied to the switches during simulation. Fig.8 and Fig.9 shows input voltage and current and output voltage during simulation. Fig.10 and Fig.11 shows the voltage across capacitor C_1 and C_2 and the voltage across the diode D_p and D_N during simulation.

3. Bridgeless SEPIC PFC Prototype

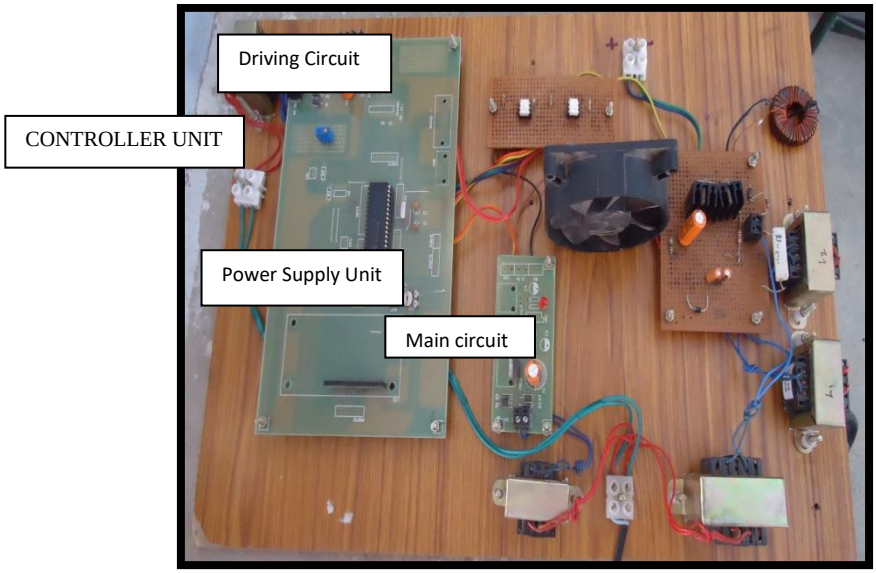

Fig.12.Hardware of Bridgeless SEPIC

Hardware circuit is shown in Fig.12.The main circuit consists of two MOSFET's, three inductors, three diodes, three capacitors. L_3 is toroidal type inductor. Two switches operate in alternate cycles with 180 degree phase shift. C_1 &C_2 also operate in alternate cycle. Output diode will combine this alternate cycle.

Fig.13. Gate signal for switch S_1

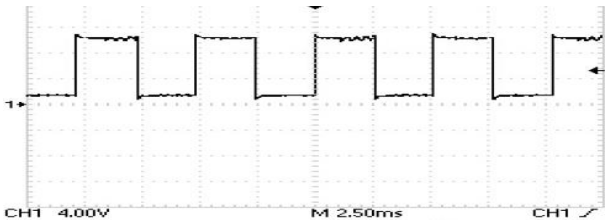

Fig. 14. Gate signal for switch S_2

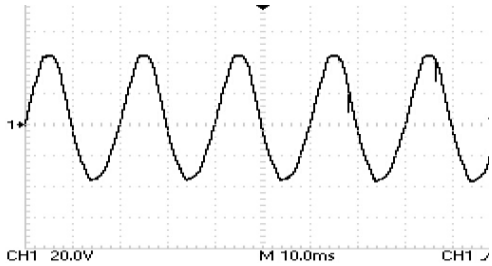

Fig.15. Prototype input Voltage obtained in DSO

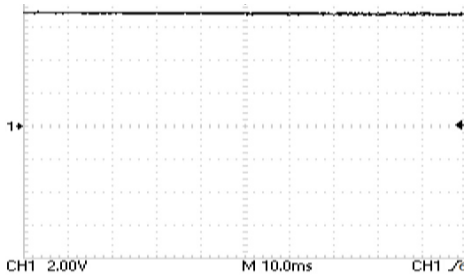

Fig.16. Prototype output Voltage obtained in DSO

Fig.13 and Fig.14. shows the gate pulse for switches in hardware circuit. Fig. 15. and Fig.16.shows the input and output voltage obtained using DSO from hardware circuit.

Table 3. Comparison of hardware and Simulation Results

Parameters		**Simulation Results**	**Hardware Results**
Input Voltage		15V	15V
Output Voltage		7.5	6.4
Load Resistance R_L		10KΩ	10KΩ
Number of Switches		2	2
Switch used		MOSFET	MOSFET(IRF 540)
Inductors	L_1	110mH	110mH
	L_2	110mH	110mH
	L_3	85mH	85mH
Input Capacitor C_1=C_2		1µF	1µF
Output Capacitor C_o		1000µF	1000µF
Switching frequency		50KHz	50KHz

Table2 shows the comparison of components used, input voltage applied and output voltage obtained in hardware and simulation circuit. Performance comparison of Conventional and bridgeless SEPIC PFC rectifiers is shown in Table3. The switching stress is less in bridgeless SEPIC PFC because of lower voltage and current across the switches. The efficiency is more compared to conventional SEPIC PFC. The THD of bridgeless SEPIC is less compared to conventional SEPIC.

Table. 3. Performance Comparison of PFC Rectifiers

Particulars	Conventional sepic	Bridgeless sepic
%THD	4.2	3.6
% Efficiency	94.5	96.1
Switch peak voltage	560	350
Switch rms current	3.3 A	2.2 A
Output diode rms current	2.1 A	2.3 A

4. Conclusion

Bridgeless SEPIC PFC circuit with closed loop control is presented. This has low conduction losses and good load regulation. The main advantage is current and voltage in input are in phase, so power loss is less. Input current distortion is low. Near unity power factor is obtained in a simple manner by the circuit operation in discontinuous conduction mode. The complexity of the control circuit is reduced. DCM operation helps power switch turn on and output diode turn off at zero-current. Line side power factor is maintained for all load.

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