Research Article

Design and Analysis of FS-TSPC-DET Flip-Flop for IoT Applications

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Abstract: The paper outlines the utmost importance of energy-efficient devices for IoT applications and recommends adual edge-triggeredTSPC flip-flop in fully-static mode at 45nm technology with low supply rail carried out in CMOS using MENTOR GRAPHICS tool.The proposed flip-flop proved to be energy efficient compared to traditional double and single edge-triggered flip-flops in terms of latency, power, the figure of merit and area for IoT applications. A comparison of two types of dual-edge triggered flip-flops are analyzed concerning the mentioned performance metrics and deduces the best flip-flop for IoT applications. Clock overlap issues are turning down in dual edge-triggered TSPC flip-flopcompared with a conventional dual edge-triggered flip-flop in full static modeand allow stringent operation at 1V supply rail thatdelivers1.14uW power, 0.60fJ figure of merit and 531.99ps latency at 45nm CMOS.

Keywords: Power, Latency, True Single-Phase Clock (TSPC), Dual edge-triggered Flip-flop (DET-FF), Figure of merit (FOM), Internet of Things (IoT).

1. Introduction

In a recentscenario,theInternet of Things (IoT) is the most emerging area in the era of healthcare and smart environments. IoT constitutes the vital components like objects & sensors. IoT devices mostly use the battery as a power source for their desired operation.It requires devices with maximum battery life, high speed and portable.The battery life is improved with a low voltage operation called voltage scaling. The speed of thesedevices is increased by minimizing un-necessary delays [1], [2]. These devices become portable by scaling down the length of the transistors to an optimum size. Several methods are utilized for low voltage operation and are achieved by sub-threshold techniques.

IoT devices utilize memory elements for data processing applications in various fields. Memory elements may be either a latch or a flip-flop. Flip-flops are the most vital components for present circuit design to store 1-bit of data. Flip-flops are sensitive to edges of the clock to perform storage operations. Besides storage, flip-flops are also used to synchronize the data flow. Hence, the synchronization is done throughout the entire clock [3]. A huge number of flip-flops are used in a regular processor, frequently many thousands. flip-flops involve an enormous part of the general circuit, decreasing power utilization has an extraordinary impact on system-level energy efficiency [4]. Particularly for energy-compelled IoT applications. Reducing power utilization in IoT integrated circuit is significant for increasing battery life. But flip-flops which are switch by every clock cycle, consume a huge part of the dynamic power in an organized system. Therefore, many experimenting works have been performed to create flip-flops with lower power utilization and better energy proficiency.

The most recommended procedure for a flip-flop is utilizing either the rising or falling edge of the clock as atrigger source for the switching operation. This kind of flip-flop is known as a Single-Edge-Triggered flip-flop (SET-FF) [1], [5], The other form of flip-flops are Dual edge-triggered flip-flops (DET-FF) use the both rising & falling edge of the clock to perform the desired operation. Utilization of both clock edges accomplishes better energy proficiency because it latches the data for both the edges. Therefore, the throughput of DET-FFis maximum than SET-FF compared at the same clock frequency. Hence, the DET-FFis proposed as an alternative sequential circuit element for low power utilization compared to SET-FF [6], [7].

SET FF & DET FF are realized by using severaldynamicCMOS logic styles like C-CMOS, Domino, N-P MOS, Dual threshold CMOS, Multi threshold CMOS, LVCMOS, TSPC logic. Of these, True single-phase clock (TSPC) logic-based flip-flopsdiminish the leakage current generated at the dynamic nodes and utilize the wide operational frequency range in the CMOS process. TSPC also performs the flip-flop operation with low power, delay and high clock speed [8] [9]. TSPC logic uses a single-phase clock to implement the latches and these latches are non-inverting. In TSPC logic, the functionality is embedded into the latch which reduces delay overhead provided by the latches.

In this paper, DET-FF's are realized by using TSPC logic because of its advantages compared with remaining logic styles. DET-FF's are implemented with TSPC by using both AND-OR logic and TRANSMISSION GATES at the output side as a MUX to produce necessary output Q. It provides a comparative analysis of both the flip-flops in terms of reliable parameters like power, latency and figure of merit (FOM). It also deduces the best DET-FF that suits IoT applications.

Meantime, a simple and widely designed technique is used for maximizing the energy efficiency in the electronic system is voltage scaling. By diminishingsupply rail voltage V_{DD}, a quadratic drop in dynamic energy utilization was observed. Hence, voltage scaling can be widely used for the less energy-constrained IoT applications.

2. Proposed Art

The proposed art entitles Full Static-True Single-PhaseClock-Dual Edge Triggered Flip-Flop (FS-TSPC-DET-FF) that acts as Data Flip-Flop (D-FF) is implemented with TSPC logic and developed in 45nm CMOS technology using AND-OR logic & Transmission gate MUXas the output drivers to provide full voltage swing at the output node Q. It also provides a compact size flip-flop for portable IoT applications [10], [11].

Data Flip-Flopsarecommonlydesigned by using latches in cascaded nature.Latches that are usually available are positive latch and negative latch cascaded together to form a flip-flop or a register. Fig 1. shows the positive and negative latches cascaded together to form a D-flip-flop with D as its input, Q as the output. The operation of the D-FF signifies that the output is identical to the input. D-FF proposed in this era uses only a single-phase clock to carry out its operation [10], [12]. It presents the desired operation on both the edges of the clock (rising & falling edges).These latches are encapsulated with theoutput drivers like AND-OR gate, transmission gate MUXthatoperatesasDualEdge Triggered – Flip-Flop (DET-FF).

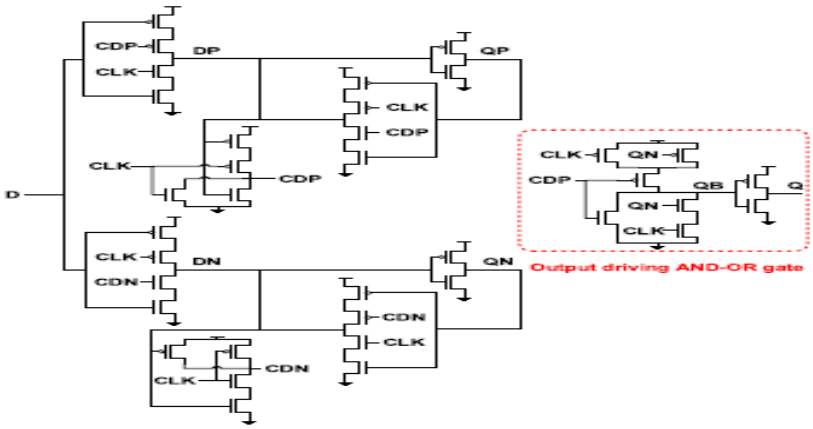

Figure 1.TSPC DET-FF with AND-OR Logic

The operations carried out in figures 1 & 2 are similar up to the output driver stage nodes QP & QN of the latches that are utilized in the D-FF. Figure 1 utilizes a clock (CLK) to accomplish the flip-flop operation. The proposed D-FF circuit uses two critical signals CDP, CDN across the positive & negative latches respectively to facilitate the desired operation. CDP, CDN are the two necessary signals generated from the NAND & NOR gates at the respective latches as in figures1 & 2. In this era, CDP, CDN is used to provide strong pull-up/pull-down for the flip-flop. Likewise, it latches the outputs QP, QN to the output node Q. From Figures 1 & 2, the nodesDP, DN, QP, QN are the inputs & outputs of the latches respectively. The outputs that are latched on to the output node Q are dispute free logic values [10], [13], [14].

The Boolean expressions for CDP & CDN [10] are expressed by using CLK, DP, DN with the help of NOR, NAND gates for positive & negative latches respectively as indicated below IN equation (1) & (2).

$$CDP=(DP+CLK)' \quad (1)$$

$$CDN=(DN.CLK)' \quad (2)$$

The critical node values CDP, CDN depends on the QP, QN values generated from positive & negative latches respectively [10].The output node Q is obtained with the help of CLK, QP & QN as stated below in equation (3).

$$Q= QN.CLK+QP.CLK' \quad (3)$$

As CLK=’0’ & D=’0’, the critical nodes are pre-charged to HIGH logic with CDP = CDN =’1’, At the same time, the output node Q holds the previous state that is located at ‘0’. As the CLK only changes its transition from ‘0’ to ‘1’ and consider ‘D’ remains uniform that results in the changes of critical nodes CDP & CDN as CDP=CDN=’0’ and latches the output node Q =’0’.

As CLK='0' & D='1', the critical nodes are pre-charged with CDP = '0' &CDN ='1', At the same time, the output node Q produces '0'. As the CLK only changes its transition from '0' to '1' and consider 'D' remains uniform that results in the changes of critical nodes CDP & CDN as CDP='0' & CDN='1' and latches the output node Q ='1'.

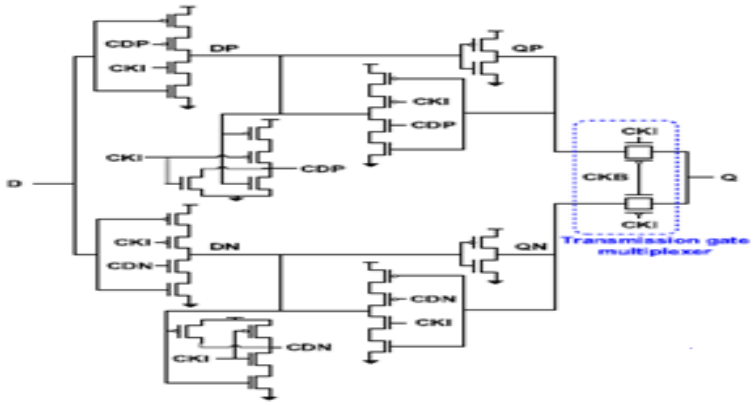

Figure 2. TSPC DET-FF with TG-MUX

The circuit proposed in figure2 operates similarly to the circuit that is proposed in figure 1 up to the output driver stage. AND-ORoutput driver stage in figure 1 is replaced with transmission-gate based MUX to latch the QP, QN outputs to the output node Q. FS-TSPC DET-FF is proposed on MUX based topologyto allow CLK & CLKI to perform the D-FF operation. CLKI is the delayed CLK to overcome clock overlap issues during the operation. The use of CLKI in the figure2 makes the circuit operate efficiently compared with figure1. CLK & CLKI are primarily used to enable both the positive & negative latches at the same time to enhance the speed. A transmission gate-basedMUX, controlled by a two-phase clocklatch the data from both the latches to output node Q with minimized constraints [10], [15].

The transmission-gate MUX selects either QP or QN based on the selection line CLKB. As CLKB ='0', the output node Q=QP. and CLKB ='1', the output node Q=QN. CLKB is the inversion of the CLK to perform latching of the data from QP, QN to output node Q without disturbing the latch operation.

FS-TSPC DET-FF implemented with AND-OR logic circuit indicated in figure1 suffers from several conslikemore power and low speed of operation during the simulation. The cons specified across AND-OR logic is diminished by transmission-gate MUX. Figure2 also overcomes all clock overlap issues that were recognized in the existing circuits.Table 1. Shows the results of different CMOS technologies for the existing circuit [10], [16].

3. Results and Discussion

This section entitles the simulations carried out in the MENTOR GRAPHICS tool, cons that are observed in AND-OR logic, pros by using transmission-gate MUX, comparative analysis of both the circuits at circuit level in terms of several parameters, like, Power, Speed, Figure of Merit, etc. It recognizes the best-proposed latch to carry out desired IoT applications.

The simulation wascarried out using the MENTOR GRAPHICS tool using 130nm, 90nm, 45nm CMOS process with V_{DD}= 1V at 27^{O}C temperature for both AND-OR logic& transmission-gatebased MUX latches are mentioned in figures 1 & 2. ELDO Simulator is used to carry out simulations to reckon the parameters like power, latency and figure of merit for each technology parameter. Simulated waveforms of the AND-OR logic & transmission-gate-based MUX latches are shown in figures3 & 4 respectively [10], [17].Figures3 & 4 represent the simulated waveforms of AND-OR logic & transmission-gate-based MUX latches that use CLK as the control signal to latch the input D to the output node Q. It is noticed that output Q of the AND-OR logic in figure3 suffers from glitches that increase the power dissipation of the latchand also degrade the output logic levels [10], [18], [19-51]. Figure4 presents the output waveform of the transmission-gate based MUX latch with glitch-free that diminishes the power dissipation and enhances the speed of operation to a great extent. The waveforms in figure3 & 4 are simulated at a 45nm CMOS process.

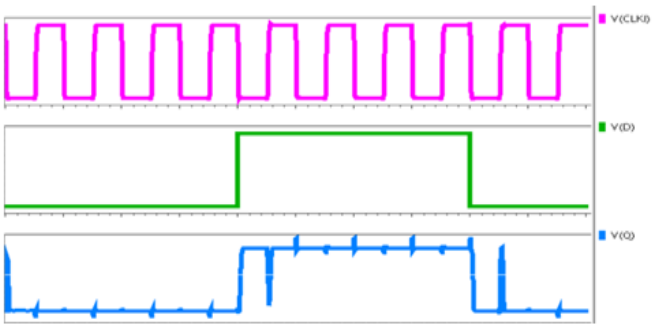

Figure 3. Simulation waveform of AND-OR logic-based latch at 45nm CMOS

It is noticed from figures3 & 5, the output logic at node Q is fully static with maximum voltage swings at logic '0' & logic '1' nodes respectively. It dictates that TSPC based circuits constitute logic'0' = 0V & logic '1' = VDD across the output nodes Q in both AND-OR, MUX based FS-TSPC DET-FF.

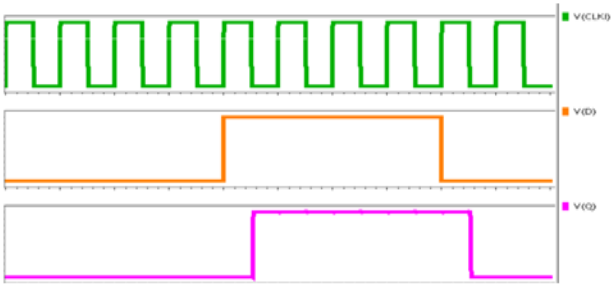

Figure 4. Simulation waveform of Transmission-gate based MUX latch at 45nm CMOS

The parametric values like power, latency & figure of merit of anFS-TSPC-DET FF implemented by using AND-OR logic-based MUX & transmission-gate-based MUX at different technology parameters are in Table 1. It is noticed that the Power, Latency & Figure of Merit is maximum at 130nm and minimum at 45nm CMOS process.

Parameter / **Technology**	**AND OR DET-FF**			**TG DET-FF**		
	Supply Voltage = 1V, Temperature = 27°C					
	130	**90**	**45**	**130**	**90**	**45**
Power (uW)	8.25	3.14	1.28	7.16	2.68	1.14
Latency (ps)	620.20	560.44	544.19	573.50	540.80	531.59
Figure of Merit (fJ)	5.11	1.75	0.70	4.10	1.45	0.60

Table 1. Different Technology Parameters

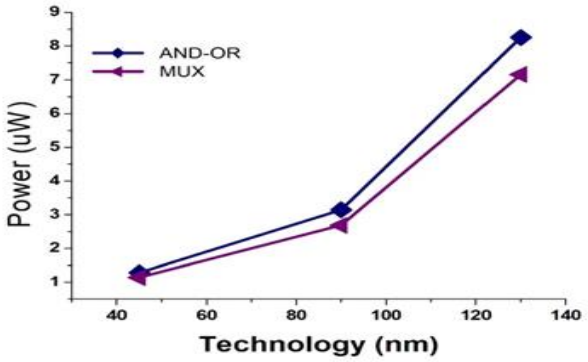

Figure 5. Graphical comparison of power with technology for FS-TSPC DET-FF

From Table1 & Figure5, Power dissipated from the latch is the average dynamic power dissipation evaluated from the waveforms using the ELDO simulator. The average dynamic power dissipation [3], [9] is evaluated theoretically by using equation (4) as

$$\mathbf{P_{avg\ dynamic} = C_L.V_{DD}^2.f} \quad \mathbf{(4)}$$

From Equation (4), C_L dictates load capacitance of the latch at output node Q, V_{DD} dictates the supply voltage of the latch and f dictates the frequency of operation for the latch.

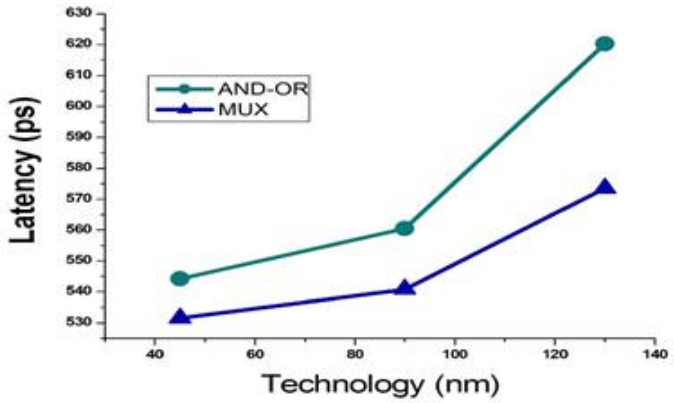

Figure 6. Graphical comparison of Latency with technology for FS-TSPC DET-FF

From Table1 & Figure6, Latency from the latch is the average delay evaluated from the waveforms between CLK & output node Q using the ELDO simulator. The latency exists only for sequential circuitsthat operate with the CLK.

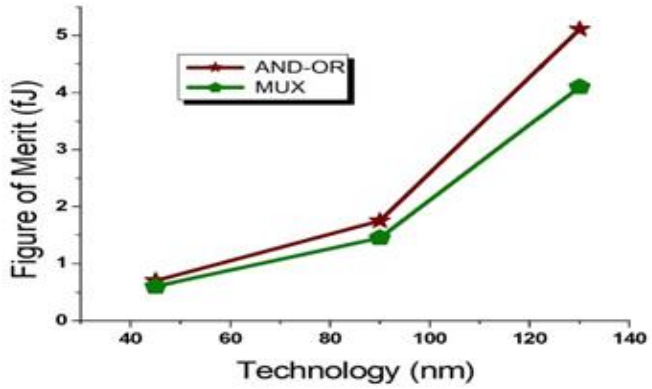

Figure 7. Graphical comparison of Figure of Merit with technology for FS-TSPC DET-FF

From Table1 & Figure7, the Figure of Merit from the latch is the average dynamic power dissipation multiplied with the Latency. Figure of Merit is evaluated theoretically by using equation (5) as

$$\mathbf{Figure\ of\ Merit\ (FOM) = P_{avg\ dynamic} * Latency} \quad \mathbf{(5)}$$

Figures 5,6,7 dictate the graphical comparison of power, latency & figure of merit with technology for AND-OR & MUX based FS-TSPC DET-FF varying from 130nm to 45nm CMOS process technology at a uniform temperature of 27^OC, frequency = 1 GHz& V_{DD} = 1V. It is noticed that several parametric values like power, latency & figure of merit are maximum for AND-OR based FS-TSPC DET-FF compared with transmission-gate MUX based FS-TSPC DET-FF at 130nm, 90nm & 45nm respectively [10], [19]. It also dictates that as the technology scales down the parameters like power, latency & figure of merit also scale down respectively.

4. Conclusion

The conclusion dictates that transmission-gate MUXbased Fully static True single-phase Dual edge-triggered flip-flop (FS TSPC DET-FF)yields low power dissipation, high speed & optimized figure of merit at the output node Q compared with AND-OR based Fully static True single-phase Dual edge-triggered flip-flop

(FS TSPC DET-FF) at a uniform temperature of 27^{O}C, frequency = 1 GHz & V_{DD} = 1V for 130nm, 90nm & 45nm technologies respectively. The transmission-gate MUXbased FS TSPC DET-FF yields optimized parametric values of Power = 1.14uW, Latency = 531.59ps & Figure of Merit = 0.60fJ at 45nm CMOS. It also dictates that transmission-gate MUX based FS TSPC DET-FF Power is diminished by 10%, Latency by 2% & Figure of merit by 14% at 45nm CMOS compared with AND-OR based FS TSPC DET-FF using MENTOR GRAPHICS tool and manifest that transmission-gate MUXbased FS TSPC DET-FF overcome clock overlap issues, furnishes voltage scaling down declares that it is best suitable for IoT applications.

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