Design and Analysis of an Artificial Neural Network Controller based UPFC Embedded with Five Level Cascaded H Bridge Inverter with SPWM and SVPWM Techniques for Transient and Dynamic Stability Enhancement of Power Systems

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Abstract: Power system dynamic and transient stability issues are answered by UPFCs [1-3] to some extent. Improvement in the performance capabilities of the UPFCs can be obtained by incorporating certain changes in the converter configurations, the PWM techniques used and the soft computing technique adopted in the designing of the controllers. Accordingly 5 level Cascaded H Bridge Inverters are used in the converters of the UPFC and PWM techniques used for the converters are Sinusoidal PWM (SPWM) and Space Vector PWM (SVPWM) techniques. A recent advancement in soft computing technique i.e., the Artificial Neural Network is adopted in the designing of the controllers. This paper emphasizes on the importance of the use of the space vector pwm (SVPWM) technique over the sinusoidal pwm (SPWM) technique. It also emphasizes on the application of an ANN technique used for controlling the different electrical parameters in the electrical network used. To observe the relative performance capabilities of an SPWM based and an SVPWM based UPFC, controlled by an ANN controller, an IEEE 5 bus system is chosen. The Performance improvement of the novel UPFC (incorporating an ANN Controller, a 5 level CHB Inverter and SPWM, SVPWM techniques), with reference to the Transient Stability and Dynamic stability enhancement is analysed. This aspect is shown by calculating the settling time for the transient power wave in the cases of faults like LG and LLL and also even when the loads are changed from normal to highly inductive and highly capacitive. The ANN Controller based UPFC helps the Power System Network to restore normalcy in a lesser time when the SVPWM technique is used than when the SPWM technique is used. To test this aspect the UPFC is connected to the IEEE 5 bus system between the buses 3 and 4. The faults LG and LLL are created near bus 4 in the line 3-4 and the load variations are done at bus number 4.The Simulations are carried out using MATLAB Software.

Keywords –UPFC, IEEE-5 BUS System, Shunt Line Faults, Power Flow Control, Cascaded H Bridge (CHB) Inverters, SPWM, SVPWM, ANN Controllers, Settling Time.

I. INTRODUCTION

The Unified Power Flow Controllers were basically proposed for real time control and dynamic compensation of the ac transmission system parameters and for obtaining more flexibility in solving the problems faced by the utilities. An earnest effort towards achieving the above goals is made here especially to improve the sensitivity of the device, the quality of output of the device, the response time of the device and also the controllability of the device by making the device to act like a self thinking machine. The Unified Power Flow Controller has two converters, one a shunt converter (converter 1), connected in shunt with the transmission network and other a series converter (converter 2), and connected in series with the Transmission Network. These two converters are connected to each other by a common DC link capacitor. The presence of a common DC link enables the transfer of real and reactive power to flow between the two converters thereby enabling the absorption and injection of voltages and currents from and to the transmission network respectively. Each of the converters can

independently generate and absorb real and reactive power at their respective ac terminals. The basic function of the Shunt converter (converter 1) is to supply the real power it can also supply or absorb reactive power. The series converter (Converter 2) provides the main function of the UPFC by injecting an ac voltage of requisite magnitude Vpq ($0 \leq Vpq \leq Vpqmax$) and phase angle δ ($0 \leq \delta \leq \delta$ max) at power frequency in series with the transmission line voltage.

II. UPFC CONFIGURATION

Terminal Voltage Regulation is done with UPFCs wherein the required voltage of change required on the Transmission line say, ΔV (Vinj) , is injected either in-phase or in anti-phase mode with the existing voltage Vo on the Transmission line.

Series Capacitive Compensation is done where the required value of voltage say, Vinj, is injected in Quadrature with the Line Current.

Phase Shifting or Transmission Angle Regulation is done by injecting a voltage of $Vinj$ in an angular relationship with Vo to get the required Phase Shift (Advanced or Retarded) in the Line output voltage without change in the Magnitude of the Line output voltage.

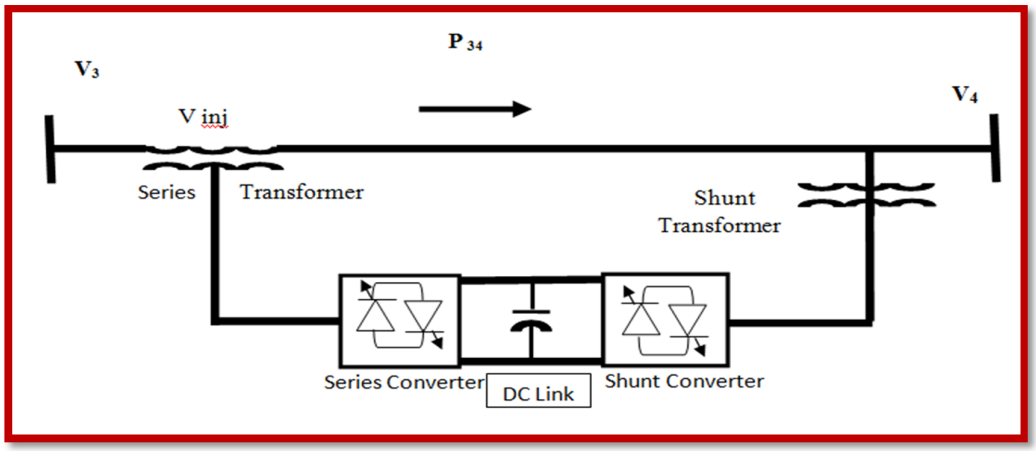

Fig.1. Five Level CHB Based UPFC for IEEE-5 Bus system connected in the line 3-4

In the explanation that follows, the importance of using the ANN Controllers, 5 level CHB Inverter, SVPWM technique, in UPFC to enhance the controlling capabilities of UPFC are clearly explained. The UPFC is connected in the system between bus number 3 and 4. The test conditions include (i) under voltage compensation (created by adding an additional 100MVAR inductive load), (ii) over voltage compensation (due to light load conditions or due to capacitive overloading created by adding an additional capacitive load of 100MVAR) (iii) transient stability enhancement capabilities when the IEEE-5 Bus system is subjected to different Shunt Faults like LG and LLL Faults at Bus No. 4.The immediate changes in the network conditions, more importantly, at the point of connection of the UPFC are detected and appropriate corrective actions are initiated by the ANN Controllers. The advantage with the CHB Inverters is made use of in improvising the Performance of the UPFC there by improving the protection levels offered to the Power System Network when the Power System is subjected to Certain Adverse and Abnormal Conditions. One of the most widely used software MATLAB is used for simulating the said test conditions.

III. THE 5 LEVEL CASCADED H BRIDGE INVERTER

One of the outcomes of the Research on the attempt to improvising the Output Voltage of an Inverter through Modifying Network/Circuit configurations of an Inverter is the Cascaded H Bridge (CHB) Inverter. The low switching voltage stress and modularity has made the Multi Level Inverters (MLIs) gain more attention. The user desired MultiLevel voltage is obtained by using different and separate voltage sources like Batteries, Fuel cells, Solar Photo Voltaic (PV) Cells, Capacitors etc., The major Advantages with Multi Level Inverters are their Minimum Harmonic Distortions in the Output Voltage, Low Electro Magnetic Emissions, High Output to Input Ratios i.e., High Efficiency and More Importantly their High Voltage Withstanding and Operating Capability and Modularity. The MultiLevel Inverters have found great applications in the areas of Drive Controls, Uninterruptible Power Supplies and Static Volt Ampere Reactive Generators (SVG).In general MLIs are divided in to three categories as Diode Clamped, Flying Capacitor and Cascaded Bridge Inverters. One of the advantages of MLIs over the Two Level Inverter is that they reduce the Common Mode Voltage causing the breaking leakage Current in Multi Drive Systems of High Power Ratings (Greater Than 250KW) based Vehicles.

The use of individual capacitors or sources at each of the H bridges makes the CHB a very strong voltage backup during voltage injection operations performs by the shunt and the series converters of the UPFC. Therefore this strong voltage support of the CHB inverter makes the CHB Inverter based UPFC a robust one. Since capacitors are used at the back to back connected DC link , the DC link will be a more stable one when compared to the support offered by single source inverters/devices.

The Circuit Topology of Cascaded H Bridge Inverter

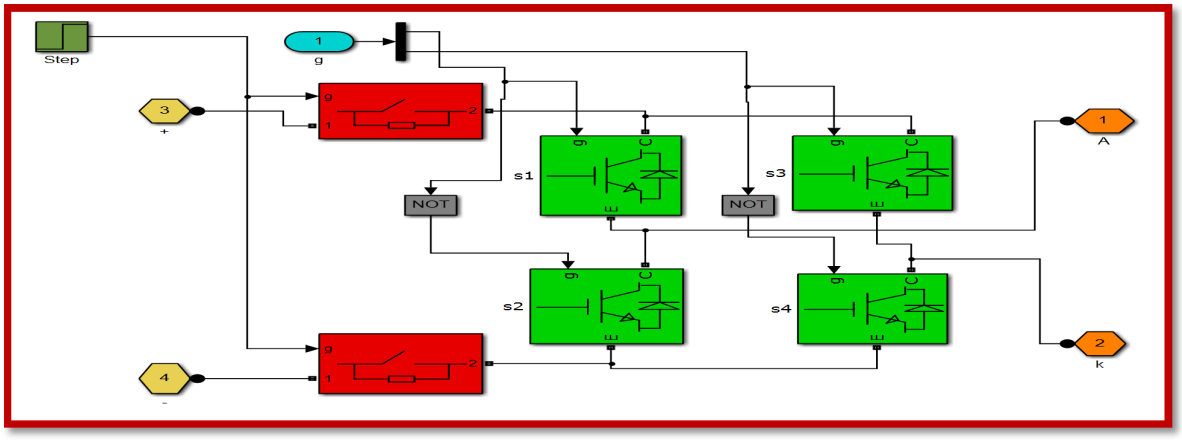

Fig.2.Basic Circuit of a CHB Inverter used in this Simulation

Figure 2 shows the basic unit of the CHB Inverter used in the simulation. It consists of four switches **S_1, S_2, S_3, S_4 .** These switches are connected to a DC voltage source via switches used for controlling the CHB during the states of transient conditions and disturbances.

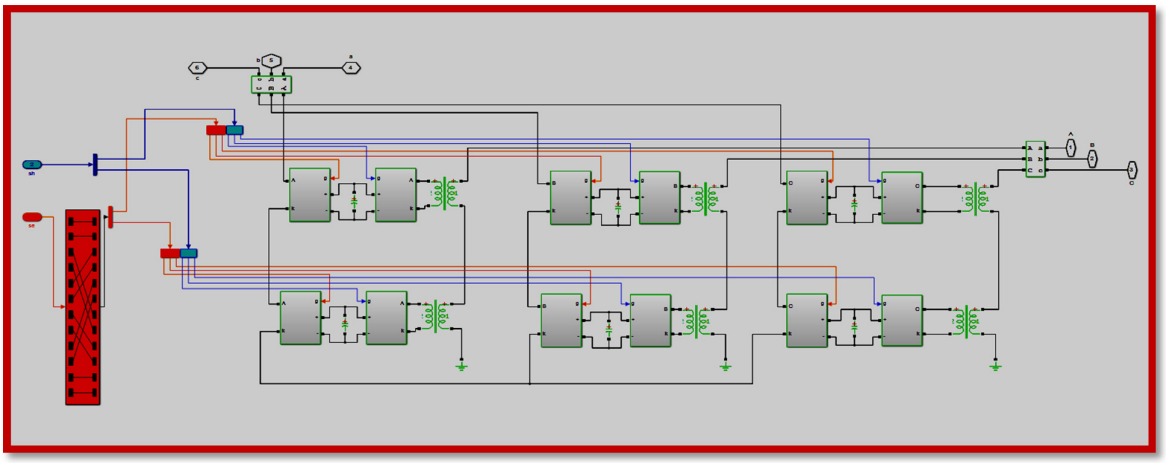

Fig.3.The 5 Level Cascaded H Bridge Inverter used in this Simulation

The equations of the CHB Inverters are written below. These equations represent the addition of the voltages at each of the H bridges .the steps in the resultant wave of the CHB are a consequence of a series addition of the voltages of the CHB individual units.

The generalized equation for an n level CHB Inverter (for one phase)

$$\boldsymbol{Va = Va1 + Va2 + Va3 + - - - - - + Van} \quad (1)$$

Where

$\boldsymbol{Va1}$, $\boldsymbol{Va2}$, $\boldsymbol{Va3}$, $- - - - -$, $\boldsymbol{Van}$ are the voltages of each of the levels of the CHB inverter .

The Fourier series equation of the output vector wave of the CHB inverter is written below and represents the complete complex form of t steppe d wave that is obtained at the inverter terminals. This is written for one phase where the other phases are 120 and 240 degrees apart for a three phase system.

$\boldsymbol{Va}\ (\omega t)$ is given by

$$\frac{4}{\pi} * \frac{\mathbf{Vdc}}{2} * \sum_{n=1,3,5,..}^{\infty} \frac{1}{n}(\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \ldots + \cos(n\theta_n)) * \sin n\varphi \quad (2)$$

Where

Vdc is the value of the DC input given to the inverter ie., the capacitor DC link voltage

n= Harmonic number

$\Theta_1, \Theta_2, \Theta_3, \ldots\ldots, \Theta_n$ are the reference switching angles for each of the levels

$$\varphi = \omega t$$

For a 5 level CHB Inverter the output voltage is given by

Van =

$$\frac{4}{\pi} * \frac{Vdc}{2} * \sum_{n=1,}^{\square} \frac{1}{n}(\cos(\theta_1) + \cos(\theta_2)) * \sin\varphi \quad (3)$$

The Modulation Index m is given by

$$m = \frac{Va1}{\frac{4 * Vdc}{2 * \pi}} \quad (4)$$

It can be seen from the equations numbered from 1 till 4, that as the level of the CHB Inverters increases the output changes i.e., the magnitude increases also the percentage closeness of the shape of inverter AC wave to the reference sinusoidal wave will be more.

IV. THE PWM TECHNIQUES

The commonly used modulation schemes for multilevel inverters are the carrier-based sinusoidal pulse-width modulation (SPWM) and the space vector modulation (SVPWM) schemes. SPWM schemes are easier to implement and provide almost the same results as far as total harmonic distortion (THD) in the output is concerned. However, from the perspective of obtaining a more Fundamental Output Waveform and Digital Implementation, the SVPWM scheme as compared with SPWM, provides flexibility in optimising the switching pattern design. For this reason most of the industrial applications prefer the SVPWM scheme.

The Sinusoidal Pulse Width Modulation (SPWM) Technique

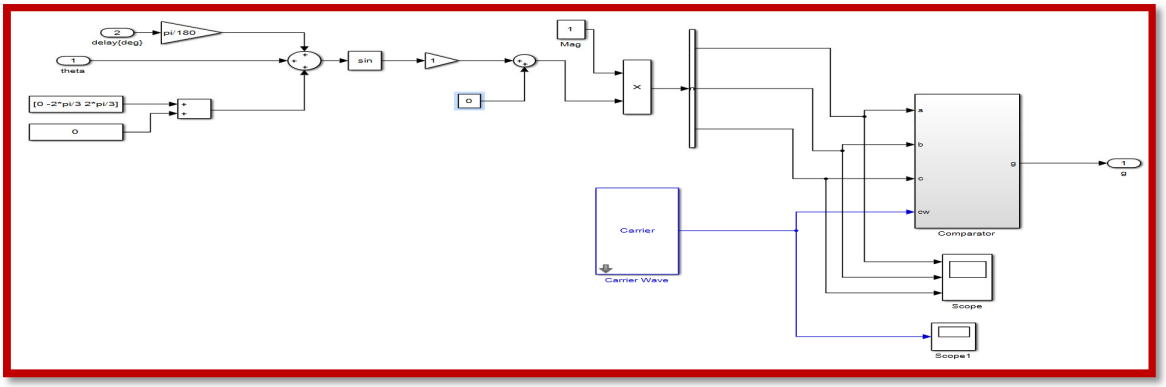

Fig.4 (a). The Sinusoidal PWM Technique Block

The figure 4(a) depicted above is the block designed to implement the sinusoidal pwm technique required for the 5 level Cascaded H Bridge Inverter.

The fundamental principle used for the SPWM technique is derived from the following equations

$V\hat{}ctrl$ =The reference sine voltage or the control voltage magnitude

Defined as

$$V\hat{}ctrl = (Vctrl) * sin(\omega t) \quad (5)$$

Vtr = The Triangular Carrier Wave,

The modulation index value is given by

$$m = (Vctrl) * sin(\omega t) / Vtr \quad (6)$$

$$where\ 0 \leq m \leq 1$$

The value of the fundamental component of the output voltage of the SPWM technique is governed by the relation

$$Vo1 = m * (Vdc/2) \quad (7)$$

Where Vdc is the value of the dc link capacitor voltage the inverter input

The SVPWM Technique

The 5 level CHB Inverter has 5 possible output voltage levels for each phase, ranging from +2E to −2E, resulting in 5^3 =125 possible space vectors for the inverter.

Of these, the numbers of fundamental space vectors are

$(3n^2 - 3n + 1) = ((3*25) - (3*5)+1) = 61$;

For our simulation because we have considered a 5 level CHB inverter we have **n = 5** for a 5-level inverter.

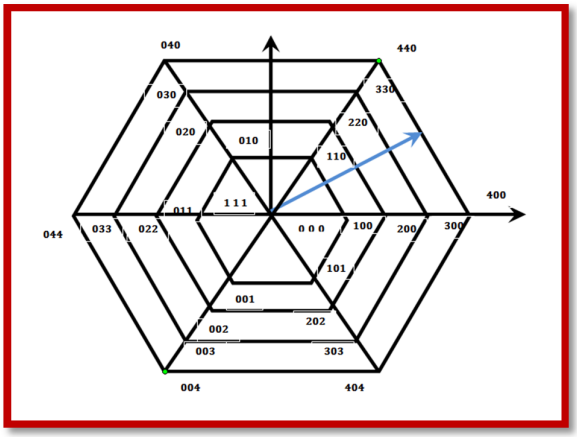

Fig.5(a) Switching States of 5 Level Cascaded H Bridge Inverter with Equal Voltages using SVPWM Technique

There are **(n – 1) = (5-1) = 4** layers and

$(n - 1)^3 = (5-1)^3 = 64$ triangles in the Space Vector Diagram.

"Depending upon the Requirement of output given by the Comparator in the Controller of the UPFC the SVPWM selects the Sector of the Voltage to be generated say V_{ref} in which the required voltage lies and Pulses are generated accordingly.

The widths of the pulses are given by the following Volt – Second balance Equations for one sector is given by

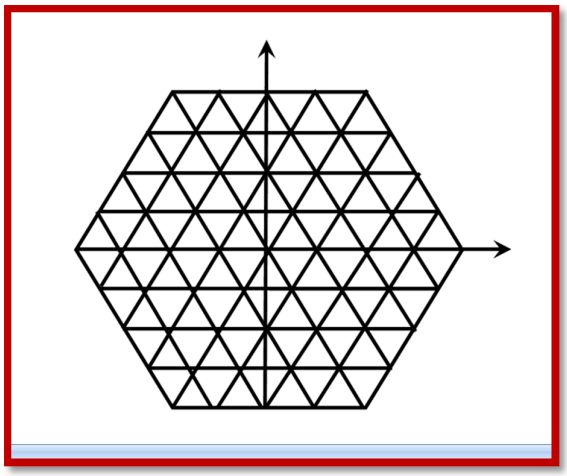

Fig.5(b) Sectorization of the switching states of 5 Level Cascaded H Bridge Inverter with Equal Voltages using SVPWM Technique

$$\boldsymbol{Vref * Ts = V1Ta + V2Tb + V0T0} \quad (8)$$

where T_s is the sampling interval; and T_a, T_b, T_0 are the respective dwell times for the vectors V_1, V_2 and V_0. The values of T_a, T_b and T_0 are given in [2] "

$$\mathbf{T_a = T_s * m * Sin(60^0 - \Theta_2)}$$

$$\mathbf{T_b = T_s * m * Sin(\Theta_2)}$$

$$\mathbf{T_0 = T_s - T_a - T_b}$$

$$\mathbf{m = \frac{\sqrt{3} * Vref}{E}} \quad (9)$$

The Series Injection Transformer is designed to a Transformation ratio of 1:1. Therefore the value of Vout of the CHB Inverter will be equal to the value of voltage injected in series with the line, Vinj

Therefore

$$\mathbf{Vref = Vinj = Vout} \quad (10)$$

V. THE CENTRAL CONTROL SYSTEM

The following figure numbered 6 details the entire control structure of the UPFC .The control structure comprises of the shunt controller controlling the DC voltage at the capacitors terminals connecting the two converters. The central controllers also has a series controller used for producing the voltage to be injected in series with the line 3-4 for balancing the voltage and also for controlling the power travelling through the line. Both the shunt and series controllers are equipped with the Artificial Neural Network (ANN) controllers which operate individually. The central control system is also included with PWM technique implementation blocks individually for the shunt and the series controllers for generating the source synchronized PWM pulse trains for the 5 level Cascaded H Bridge Inverters. Initially the SPWM technique is used and then it is replaced by the SVPWM technique for comparing the UPFC's performance.

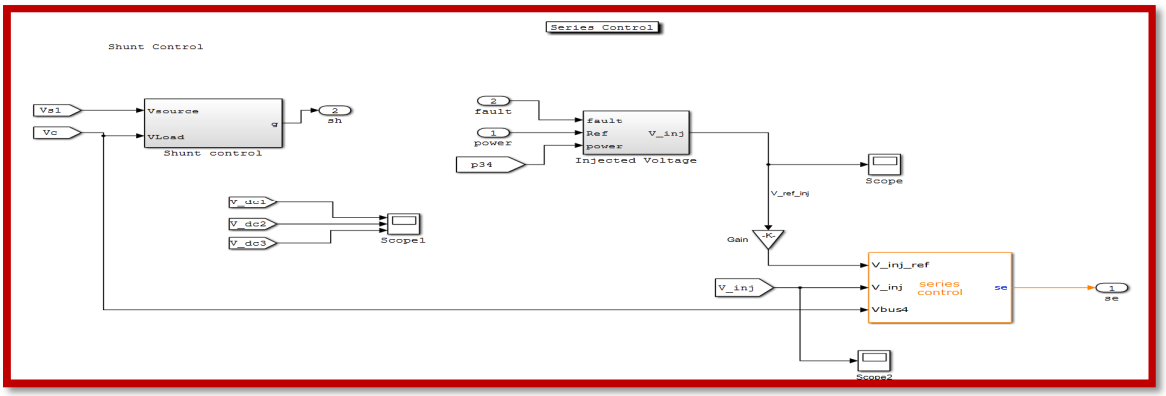

Fig.6. The Central Control System Comprising of the Series and Shunt Controllers where the SPWM and the SVPWM blocks are incorporated. It also has the Pulse Generator block.

VI. THE ARTIFICIAL NEURAL NETWORK (ANN) CONTROLLER(S)

The Artificial Neural Network controller of the shunt converter takes into consideration the voltage and current conditions on the line 3-4 and the dc voltage across the capacitors at the dc link between the two converters. The inputs also include the reference voltages to be maintained on the line 3-4 where the UPFC is connected and where the test conditions are executed. As soon as the test conditions are initiated the error value (reference value – measured value) is processed for sterilization and range testing. This error is fed to the ANN system where proper weights and bias are calculated and are added in layer 1 and layer 2, shown in figure 6, to process the output using the tansig transfer function method defined in equation 13 given below. The output is properly processed through the PID controller system and discretized to get the value of angle in degrees. This angle is input to the control system and pulse generator block, shown in figure 7, wherein the process of producing the firing pulses is executed. A sinusoidal wave with the reference angle specified by block 7 is generated and is compared with a triangular wave in case of SPWM technique and the reference angle is used to produce a pulse train for 5 level Cascaded H Bridge Inverter. For the case of the SVPWM technique a program is written using the MATLAB function block which coordinates with the other Simulink blocks.

The operation of ANN in the series converter controller will be on similar line to the ANN controller in the shunt system but with a difference that the series control system takes input the reference power values and continuously measured values of power on the line 3-4.The comparators in the series controller calculate the error and processes through the double layer 1 and layer 2 of the ANN system, to control the value of direct injected to be produced by the series controller by way of producing appropriate firing angle control technique.

The weight adjustments in the ANN controller in layer 1 are done using the following equations

The weight function for an input x

$$\boldsymbol{Wfcn(x)} = (\boldsymbol{w1} * \boldsymbol{x1} + \boldsymbol{w2} * \boldsymbol{x2} + \boldsymbol{w3} * \boldsymbol{x3} + - - - - + \boldsymbol{wn} * \boldsymbol{xn}) \quad (\mathbf{11})$$

for an n numbered input system

A proper bias is added depending upon the requirement given by the following equation

$$x' = Wfcn(x) + bias \quad (12)$$

The tansig function used

$$F_{tansig} = \frac{Gain}{e^{-2x'}+1} - constant \quad (13)$$

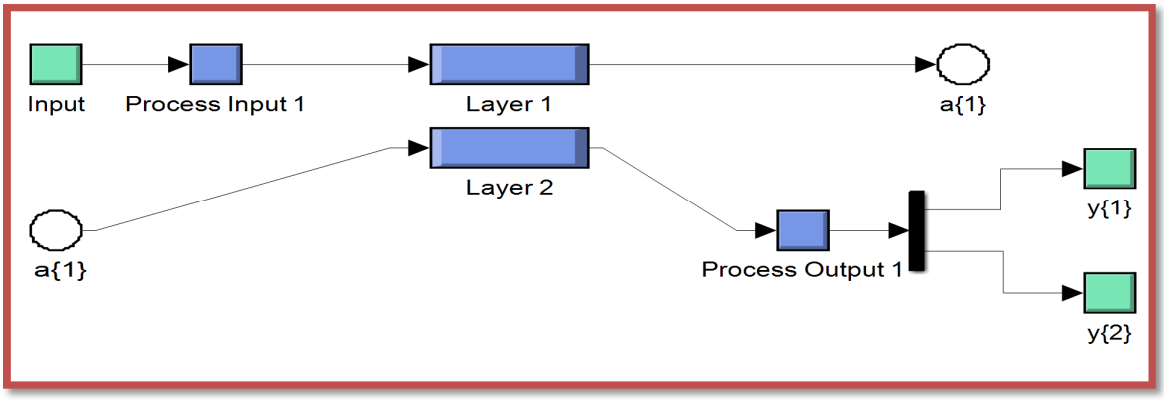

Fig.7 (a).The layer structure of the ANN Controller

The above figure 7 (a) shows the layered structure of the ANN system. The inputs error and change in error are fed s inputs to the ANN controller. For a Shunt controller the inputs are the reference voltage and the measured voltage at bus number 4 of the IEEE 5 bus system. And for the series controller the inputs are the reference value of active power and the measured value of power in the line 3-4 of the IEEE 5 bus system

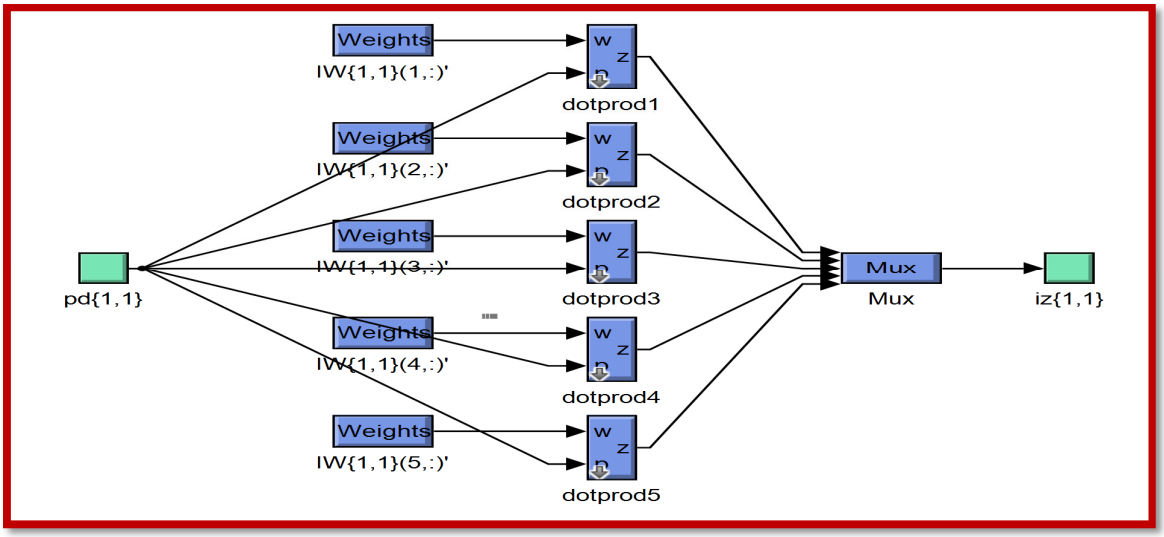

Fig.7 (b). The Internal Structure of the ANN Controller

Figure 7 (b) shows the internal structure of the internal layers which process the data continuously fed to it during the process of simulation. The inputs are processed in accordance with the equations 11 , 12 and 13.

For a shunt controller

$$e = V_{ref} - V_{meas} \quad 14$$

$$\Delta e = d\,(V_{ref} - V_{meas}) \quad 15$$

For a series controller

$$e = P_{ref} - P \quad 16$$

$$\Delta e = d\,(P_{ref} - P) \quad 17$$

VII. THE TEST SYSTEM and THE TEST CONDITIONS

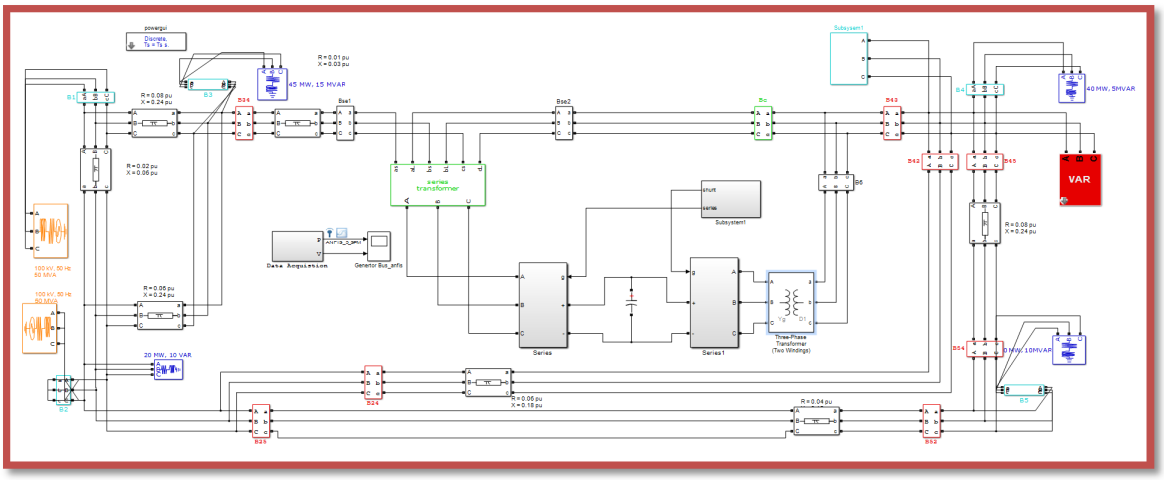

Fig.8 Simulink diagram of the complete IEEE 5 bus system connected with a 5 level CHB inverter based UPFC

The test system chosen is an IEEE 5 bus system. The system consists of 5 buses denoted from B1 to B5, coloured in cyan. Two generators are present in the system at bus numbers 1 and 2 each rated with 50MVA and 100KV. The load at bus 2 is 20MW + j10MVAR (inductive) at bus 3 is rated as 45MW + j15MVAR inductive, at bus 4 it is 40MW+ j5MVAR (inductive), at bus 5 it is 60MW+j10MVAR (inductive). The details of the line impedances are illustrated in the appendix. The above figure 8 gives an exhaustive description of the IEEE 5 bus system. It can be clearly seen that a 5 level CHB inverter based UPFC is connected between the buses 3 and 4. All the test conditions proposed are executed in the line 3 - 4 i.e., the inductive over loading and capacitor over loading conditions are created at bus number 4 between the time intervals 30 to 30.5 s and 35 to 35.5 s respectively. Shunt faults are created in the line 3 - 4 near bus number 4, which are explained in detail in the results and discussions section.

VIII. SIMULATION RESULTS and DISCUSSIONS

The complete test conditions described in the above VII section are simulated and the results are discussed in detail in this section

(i) The complete power wave

The following figure 8 shows the complete pattern of the power wave in the line 3 – 4 when the line is subjected to inductive overloading, capacitive overloading, and shunt faults. The detailed analysis pertaining to every test condition is explained in the sessions to follow.

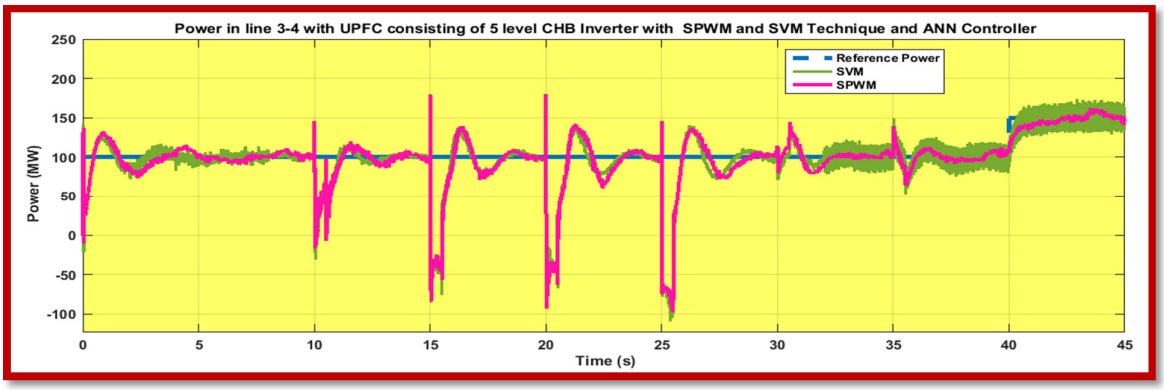

Fig. 9. The Complete Power Transferred through the Line 3-4 under different Test Conditions Using ANN Controller and SPWM and SVPWM techniques

(ii) The initial power swing

The following figure 10 indicates the influence of the 5 level CHB inverter based UPFC in supporting generators by way of injecting additional power in the line 3-4 in reaching the designated power level of 100MW from initial state when SPWM technique is used and when the SVPWM technique is used by the converters. It can be clearly observed that the power wave in the line 3 – 4 when a SVPWM technique used makes less oscillations and also reaches the designated 100MW mark in a lesser amount of time than the one with SPWM technique. With SVPWM technique the power wave takes **6s** to reach the stable state while the one with the same ANN controller and SPWM technique UPFC takes **8.0**s to reach the stable 100MW mark.

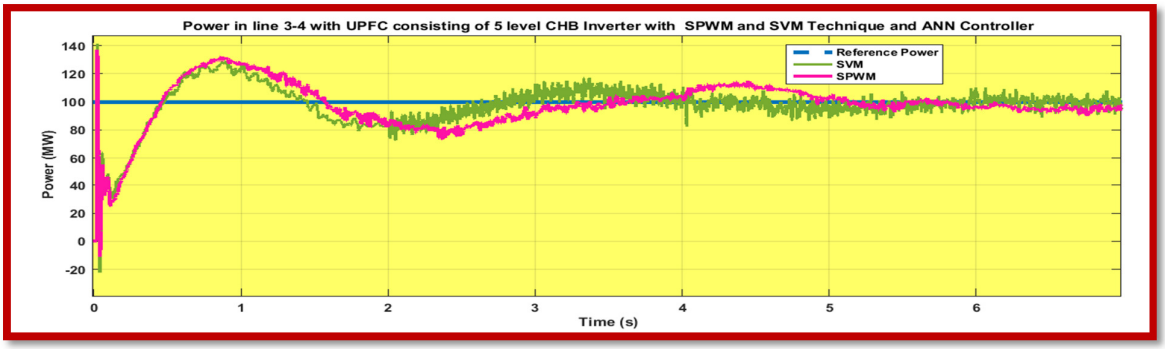

Fig.10. The Initial Power Swing through the line 3-4 using ANN controller and when SPWM and SVPWM techniques are used

(iii) Single line to ground (LG) fault in line 3 - 4 near bus 4

An LG fault is created in the line 3 – 4 near to the bus number 4 at 10th second and lasts up to 10.5 seconds.

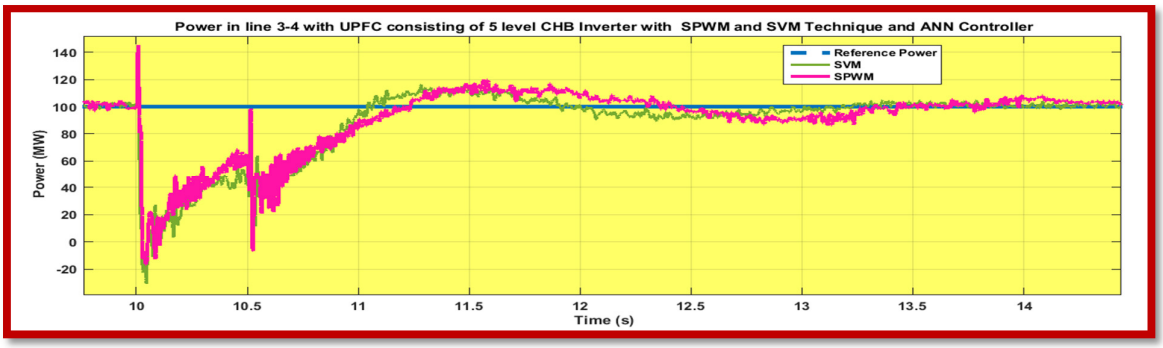

Fig.11. The Power Transferred through the Line 3-4 during LG fault conditions using SPWM and SVPWM techniques and an ANN controller

As soon as the fault is initiated the shunt and the series controllers initiate their respective corrective actions wherein the shunt controller adjusts the DC link voltage and the series controller the voltage to be injected by the series converter. But the capability of the UPFC when a 5 level CHB Inverter using SVPWM technique is more than when the SPWM technique is used. This fact is proved from the response time and the settling time depicted in the figure numbered 11.The time taken by the power wave to get settled at the normal / stable 100MW level from the point of initiation of fault is at **13.1 seconds with SVPWM** technique and it is at **13.4 seconds with SPWM technique**.

(iv) Triple line fault

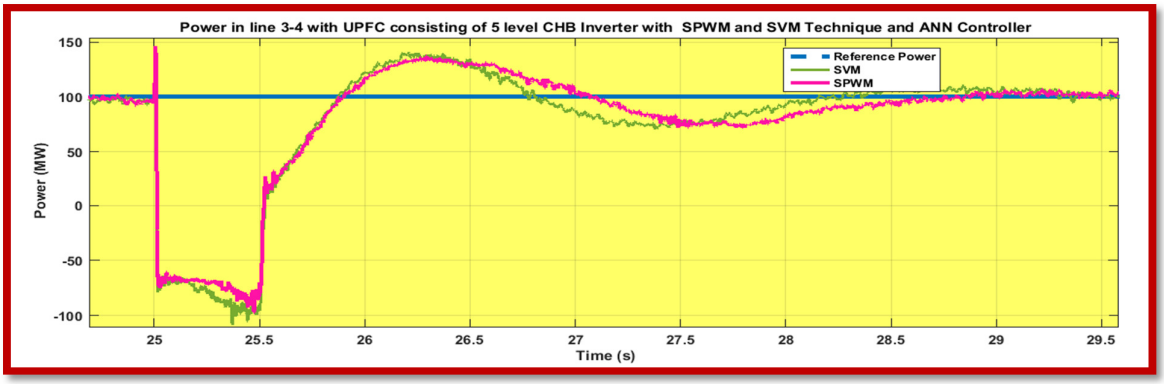

Fig.12. The Power Transferred through the Line 3 during LLL fault conditions using SPWM and SVPWM techniques and an ANN controller

Very similar to the LG fault conditions discussed above, an LLL fault is created in the line 3 – 4 near to the bus number 4 at 25th second which lasts up to 2**5.5** seconds. As soon as the fault is initiated the shunt and the series converters are initiated by the ANN controllers in the two converters. As can be seen from the figure 12, the capability of the UPFC when a 5 level CHB Inverter with SVPWM technique is used in the UPFC is more than that when the 5 level CHB Inverter with SPWM technique is used. The time taken by the power wave to get settled at the normal / stable 100MW level from the point of initiation of fault is at **28.1 seconds with a SVPWM 5 level CHB** Inverter and when a **5 level SPWM CHB** Inverter is used it is settling at **28.4 seconds**

(v) Voltage sag conditions due to inductive overloading at bus number 4

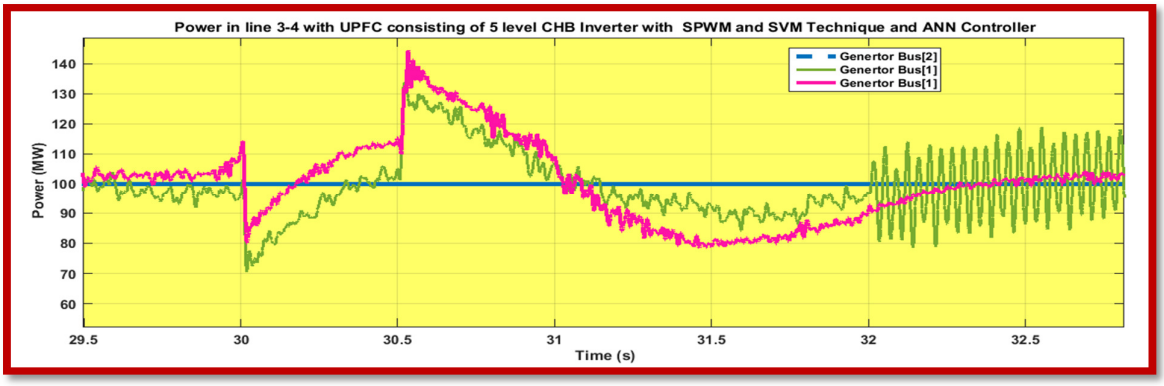

Fig.13. Power transferred through the line during Sag i.e., INDUCTIVE OVERLOADING

The capability of the UPFC for stabilizing the power system oscillations due to dynamic changes in the loading conditions is tested. Apart from the existing load of (40MW + j15MVAR) inductive at bus number 4, an excess inductive load of 50 MVAR is added at the 30th second .The sudden dip and the successive oscillations made by the power wave in line 3 - 4 can

be witnessed from the following figure 13 starting from the 30th second. These oscillations are successfully sustained by the ANN controller based UPFC when a 5 level CHB inverter using SVPWM technique and a 5 level CHB inverter using SPWM technique used, but with different settling times. The UPFC while using **SVPWM** technique brings the power wave to settle at 100MW targeted value at **32.1 seconds** and while using **SPWM it settles at 32.3 seconds.**

(iv) Voltage swell conditions due to capacitive overloading at bus 4

To test the capability of the UPFC for stabilizing the power system oscillations due to capacitive overloading, the loading conditions at bus number 4 are altered. Apart from the existing load of (40MW + j15MVAR) inductive, an excess load of 100 MVAR capacitive is added at the 35th second. The sudden swell and the successive oscillations made by the power wave in line 3 - 4 can be witnessed from the figure 14 starting from the 35th second.

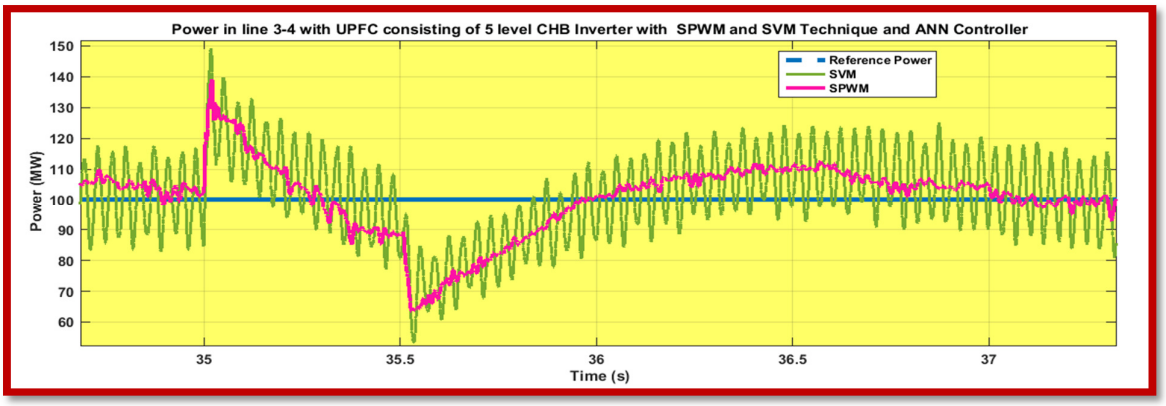

Fig.14. Power transferred through the line during Voltage Swell i.e., CAPACITIVE OVERLOADING

These oscillations are successfully sustained by the ANN controller based UPFC when a 5 level CHB Inverter is used in the UPFC but with different settling times when SVPWM and SPWM techniques are used. The UPFC using SVPWM technique makes the power wave to settle at 100MW targeted value at **36.9 seconds** and when SPWM technique is used it takes **37 seconds.**

Table 1 : RESULTS TABULATION

S.No	Type of Disturbance	Duration of disturbance in Seconds (Exact Time)	Settling time in seconds (exact time) ANN CONTROLLER	
			SPWM	SVPWM
1	Initial Swing		8	6
2	Line to ground fault	0.5 (10 to 10.5)	13.4	13.1
3	Three Phase faults	0.5 (25 to 25.5)	28.4	28.1
4	Voltage Sag	0.5 (30 to 30.5)	32.3	32.1
5	Voltage Swell	0.5 (35 to 35.5)	37	36.9

The above table 1 consolidates the settling times of the power waves in the line 3-4 of the IEEE 5 bus system. It can be observed that the settling times of the power wave are lesser i.e., settles at lesser times when a Space Vector Pulse Width Modulation technique based UPFC is used than when a Sinusoidal Pulse width PWM technique is used. It can also be observed that the faults created in the line are at close regular intervals. In general, the voltage and current waves thereby the active and reactive powers, in any system when subjected to a fault takes large times to settle to normalcy after the fault is cleared. But with the help of a UPFC it takes lesser times. If proper controlling techniques like ANN technique is used and if the UPFC's converters are designed using advanced Multi Level Inverter like CHBs and uses advanced Switching techniques like the SVPWM then the performance of the UPFC improves.

IX. CONCLUSIONS

It can be concluded that the UPFC embedded with an ANN controller with an SVPWM technique has a faster response rate. Also the vulnerability to oscillations during the controlling state is more when SPWM technique is used. This is because of the fact that the SPWM technique uses approximate values or large intervals of pulse widths when compared to the SVPWM technique. The replication of the desired Vctrl in case of SPWM or Vref in case of SVPWM , though both are to be produced by the Series Converter (where in actual Vctrl =Vinj = Vref) is more accurate with SVPWM technique. Also the computation time required by the SPWM technique is more than the SVPWM technique. This Phenomenon can be observed from the fact that the Settling Time for Restoration of Normalcy during the occurrence of Different Kinds of Disturbances, like Voltage Sag, Voltage Swell or Faults like LG and LLL is lesser when SVPWM technique is used

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APPENDIX

IEEE-5 Bus System

NUMBER OF LINES = 7
NUMBER OF BUSES = 5

In all these BUS DATA's type-3 indicates slack bus, type-2 indicates PQ / load bus, type-1 indicates PV / generator bus.

LINE DATA

SB	EB	R (p.u)	X (p.u)	Ys	Tap
1	2	0.02	0.06	0.03	1
1	3	0.08	0.24	0.025	1
2	3	0.06	0.18	0.02	1
2	4	0.06	0.18	0.02	1
2	5	0.04	0.12	0.015	1
3	4	0.01	0.03	0.01	1
4	5	0.08	0.24	0.025	1

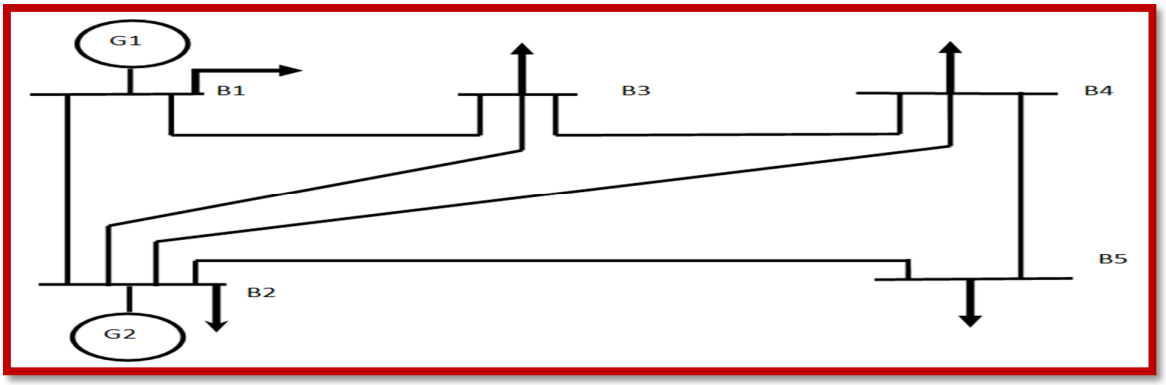

Figure : Line Diagram of the IEEE 5 Bus System

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