Implementation of Wallace Tree Multiplier Using 8:4 Compressor

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ABSTRACT:
Multipliers are prime scheme implementation of Microprocessors, VLSI and Embedded Systems. Regrettably, Multipliers are designate by compound function represent and constitute one of the supreme power consuming digital blocks. Estimate computing is an Emerging trend in VLSI design. Now a day the Multiplier is a vital role in most research and development areas. In this paper, the Implementation of Wallace tree Multiplier using 8:4 Compressor is done. The multiplier design will be made by 8:4 Compressor that reduces the power consumption than the optimized compressor design. The proposed 8:4 Compressor is implemented using AND and OR gates.

Keywords: Multiplier, 8:4 Compressor, Optimized Compressor, AND-OR gates.

I.INTRODUCTION

Many computational operations are Multiplication is widely used, without multiplication it's not possible. To design efficient multiplier is impart consuming less power and reduce delay. In the modern world quick response of multiplier is used in VLSI design technique and contemporary computing processor. However, in numerous applications presume digital signal processing and multimedia, compel and fault less estimation are not always imperative, may this results are errors unavoidable but mean while results acceptable accuracy [1]. The older Multiplication technique was normally executed by repeated addition, shifting functioning operation. Various types of multiplier are available these are Combinational multiplier, Sequential multiplier and Wallace tree multiplier [2][3]. After analyzing various multipliers technique, Array multiplier is identified that which consumes more power and delay while Booth multiplier occupies large area consumes less delay. Example for the effective parallel multiplier is Wallace tree multiplier. The implementation of full and half stage of adder is reduced and fast multiplier method getting through Wallace tree multiplier. Compressors are one of the best effective dominant of high speed multipliers [4]-[10]. The minimum feasible energy dissipation is furnishing an advanced computation in partial products at a tariff. The cause for evident predilection of compressors is that it has leads in terms of power, delay and speed.

II.EXISTING METHOD

The method of a four partial products which compressed two partial products done by the combinatory devices of 4:2 compressor [3] [5]. The structure of 4:2 compressor is shown in Fig.1.(a). Giving five input of the 4:2 compressor are X1, X2, X3,X4, C_{in}; and bring out three outputs Sum, Carry and $C_{out.}$ The first compressor output C_{out} is the input of second compressor.

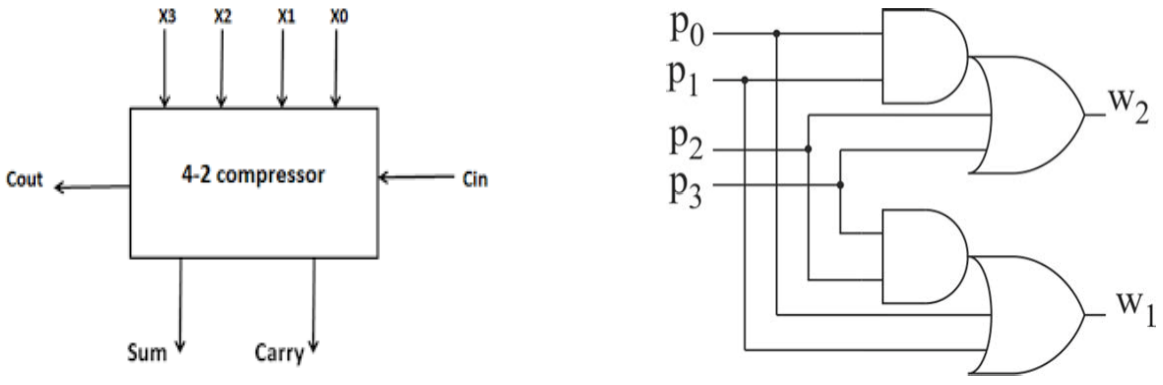

Fig.1. (a) 4:2 Compressor diagram (b) Gate equivalent model of 4:2 compressor

The gate equivalent model for AND-OR gate based configuration of 4:2 compressor is shown in Fig.1.(b). It shows that the inputs p_0, p_2, are first AND then OR with the inputs of p_2 and p_3. So that we get the output as W_1. Again the inputs p_2 and p_3 are AND then OR with p_0 and p_1 respectively. So that we get the output as w2 respectively. The AND-OR gates are used to minimize the circuit complexity because their operations are easy to understand.

The concept used the Wallace tree is to generate a largest compatibility among their carry save adders. The approach of this adder at each stage takes in three operand and produce two results, reducing the number of outputs by a factor of 1.5. The total number of stages needed is calculated to be [log $_{1.5}$(N/2)]. Final addition is carried out when there are only two outputs left, and by a carry propagate adder [3].

The method of 4:2 compressor technique having some following draw backs, these are high truncation error, its increase the delay time due to speed of multiplier is low and less accuracy level. To overcome the above disadvantages we have go for the proposed method dual quality of 4:2 compressor i.e. 8:4 compressor in multiplier.

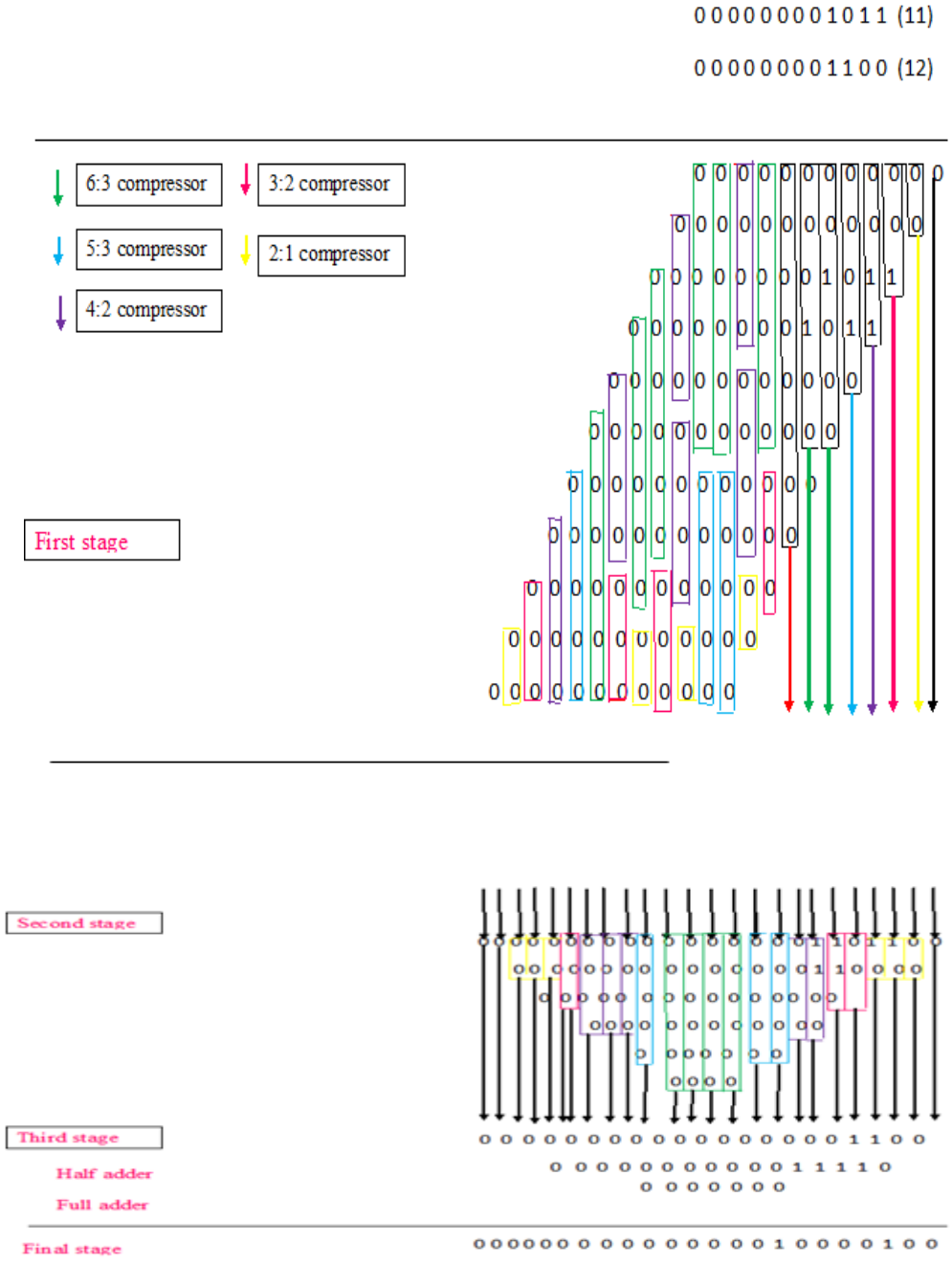

Fig.2. Existing compressor multiplier technique

III.PROPOSED METHOD

The proposed method uses the dual quality of 4:2 compressor i.e. 8:4 compressor. The use of 8:4 compressor in multiplier is that the consumption of power in a multiplier is important in any digital applications. The 8:2 compressor provides parallel addition of input bits. Hence the speed of addition operation can be improved. Varieties of multiplier available in that a fast multiplier namely Wallace tree multiplier is used. By replacing half and full adder using compressor should definitely increase the speed performance. To apply higher order compressor is develop multiplier speed tremendously improved. The proposed 8:4 AND-OR based configuration is shown in Fig.3.

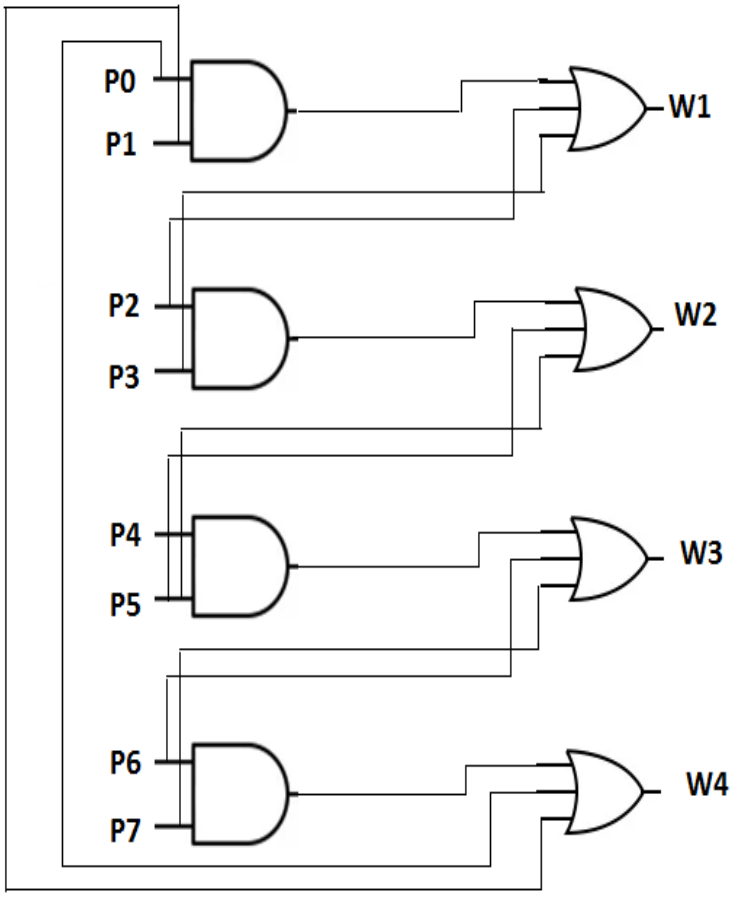

Fig.3. AND-OR gate based configuration of 8:4 compressor

The same operation as done in 4:2 compressor done in 8:4 compressor. As the proposed compressor is implemented in Wallace tree multiplier so that the amount of power consumed by any digital circuit is less compared to other conventional multiplier.

The tree based multiplier method is improver version of modified term is called Wallace tree multiplier. For the reduction phase Wallace tree multiplier use full adders, half adders. The Wallace tree multiplier is an best short method of hardware applied and effective techniques, that multiplies two integers, proposed by an Australian computer scientist Chris Wallace. For unsigned multiplication, up to n shifted copies of the multiplicand are added to form the result [5][10].

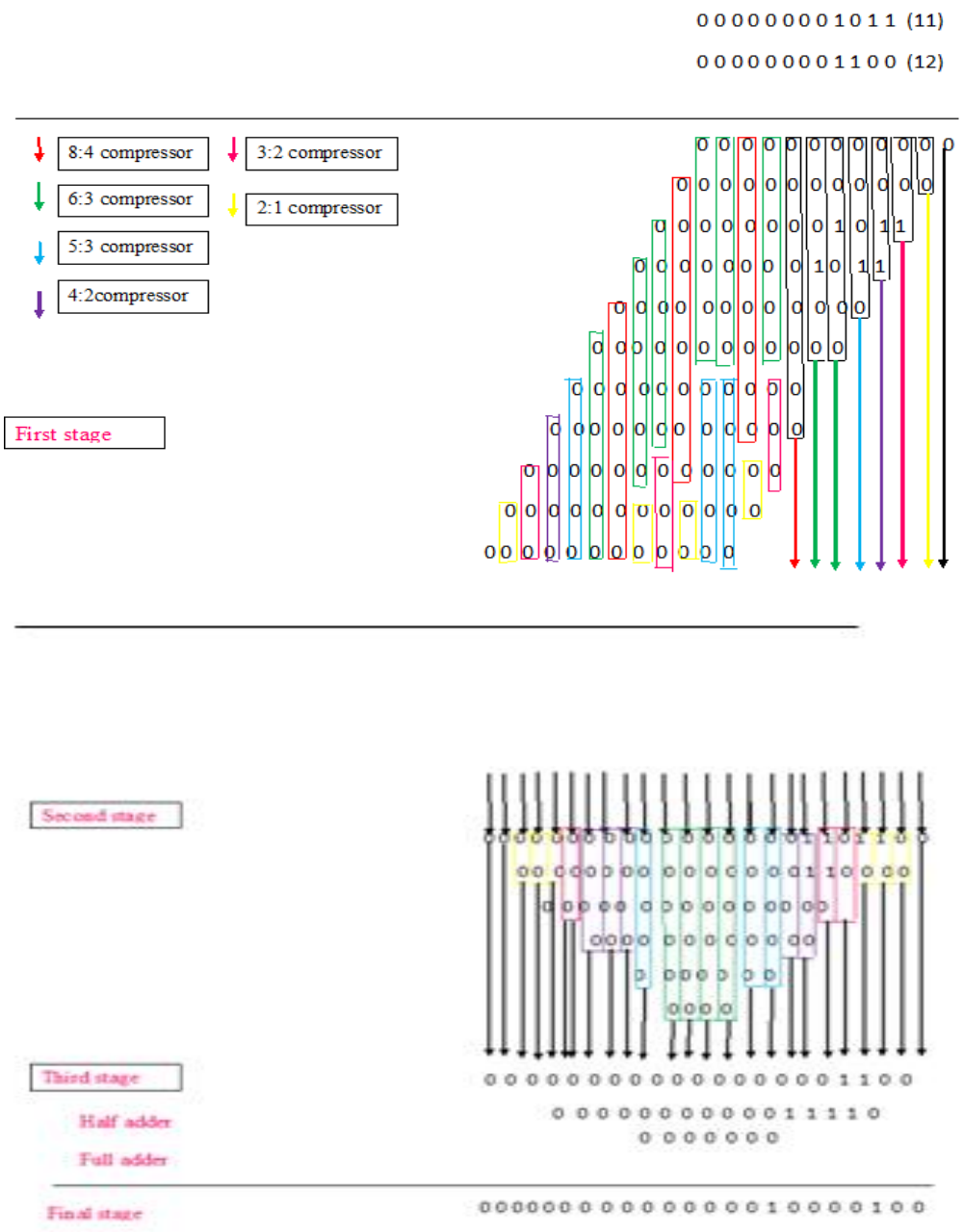

Fig.4. Proposed compressor multiplier technique

Compare to the existing method of 4:2 compressor technique draw backs are fulfill the 8:4 compressor techniques, The proposed compressor method consume low power, high accuracy and reduce the partial products and very high efficiency. Finally reduce the partial products in Wallace tree multiplier, which hug increasing of speed of the multiplier. This gives better performance compared to conventional multiplier.

IV.RESULT

The main block of multiplier is Full and Half adders section. Here the section is replaced with compressors. The 4:2 compressor simulation is done in Xilinx 14.3 version and the results are verified. Fig.5. (a).shows the output of 4:2 compressor.

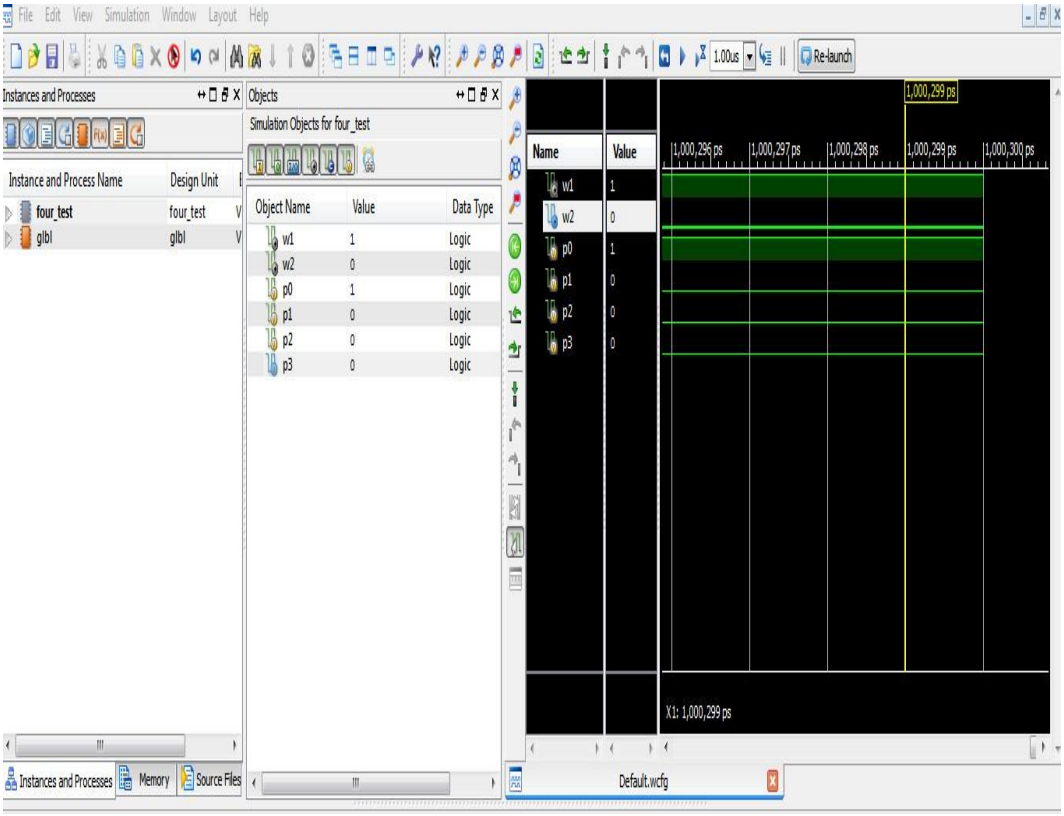

Fig.5.(a) output of 4:2 compressor

The output of 12x12 Wallace tree multiplier using 4:2 compressor is shown in Fig.5.(b).

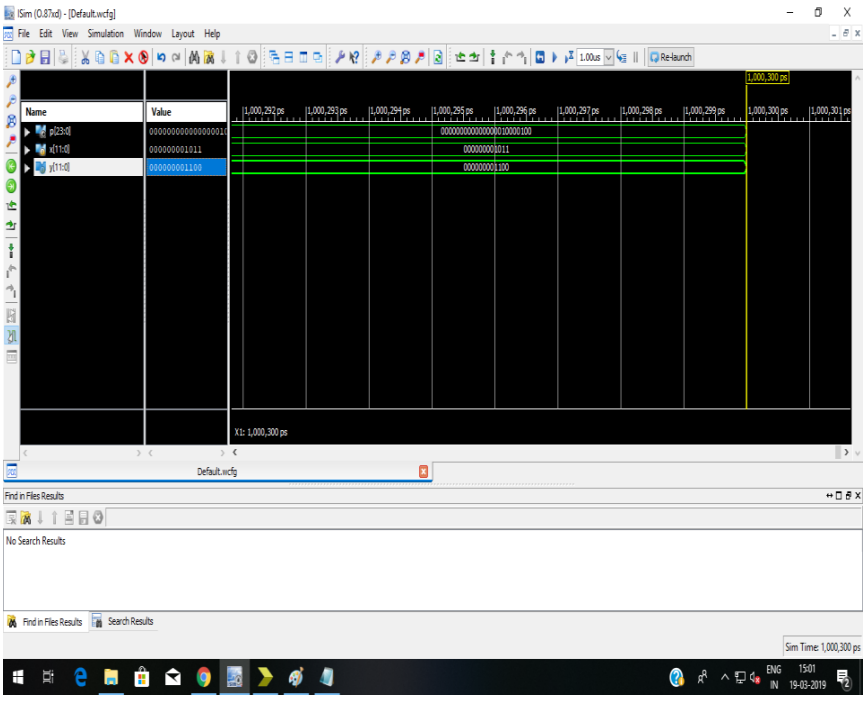

Fig.5.(b) Simulation result of 12x12 Wallace tree multiplier using 4:2 compressor

Similarly, the output of 8:4 compressor is also implemented in Xilinx 14.3 and the results are verified. Fig.6.(a) shows the output of 8:4 compressor.

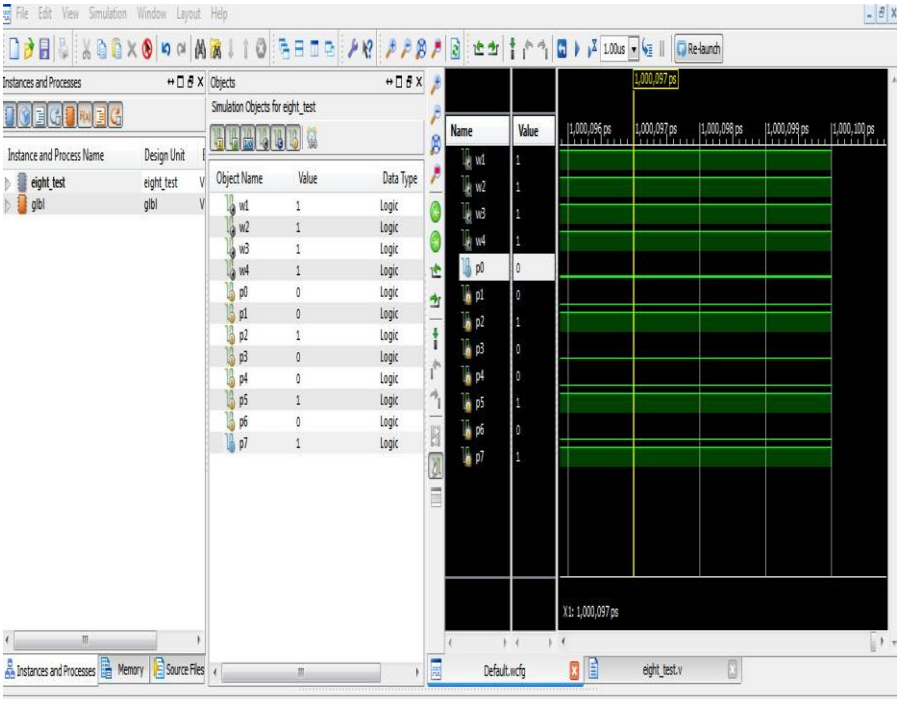

Fig.6.(a) output of 8:4 compressor

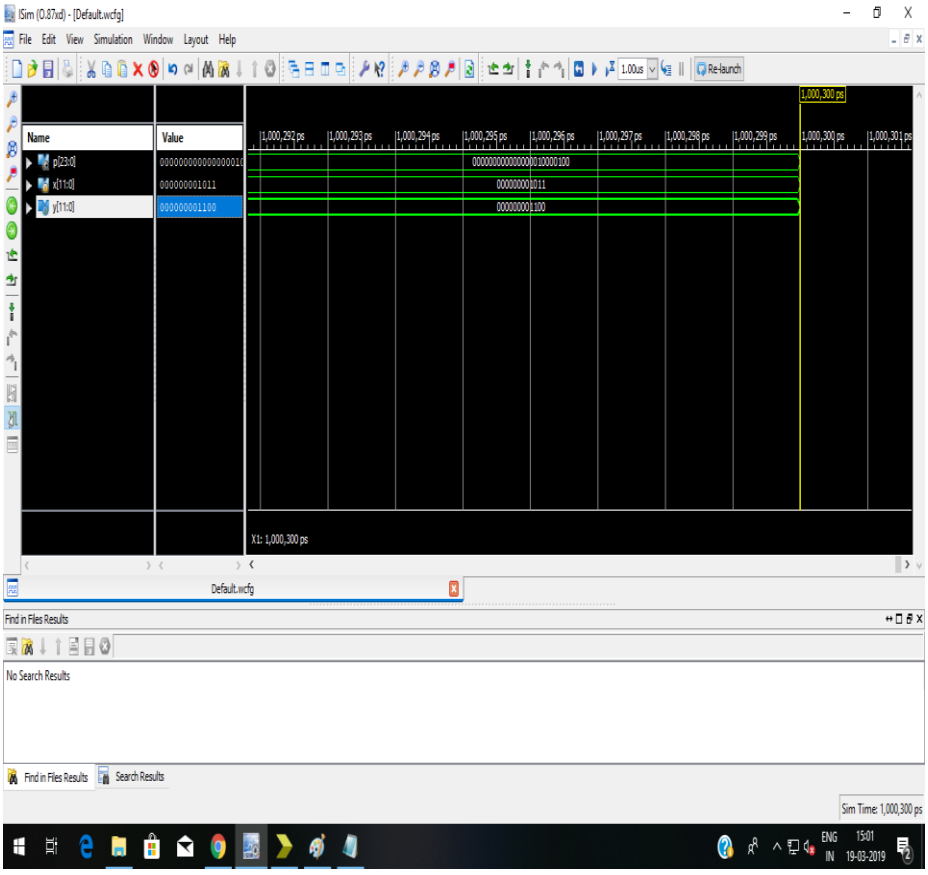

Fig.6.(b) Simulation result of 12x12 Wallace tree multiplier using 8:4 compressor

The below table shows the Area analysis of both existed and proposed system. A 4-to-1 multiplexer can be efficiently implemented in a single family slice by using dedicated components called MUXF's. The six input signals (four inputs, two select lines) use a combination of two LUTs and MUXF5 available in every slice.

Table1. Area Analysis of 4:2 and 8:4 compressor

Technique	No. of 3 input LUTs	Muxf5
Existing	61	4
Proposed	50	3

The below table shows the Delay analysis of both existed and proposed system.

Table2. Delay Analysis of 4:2 and 8:4 compressor

Technique	Delay (ns)
Existing	17.739
Proposed	17.127

The below table shows the Accuracy analysis of both existed and proposed system.

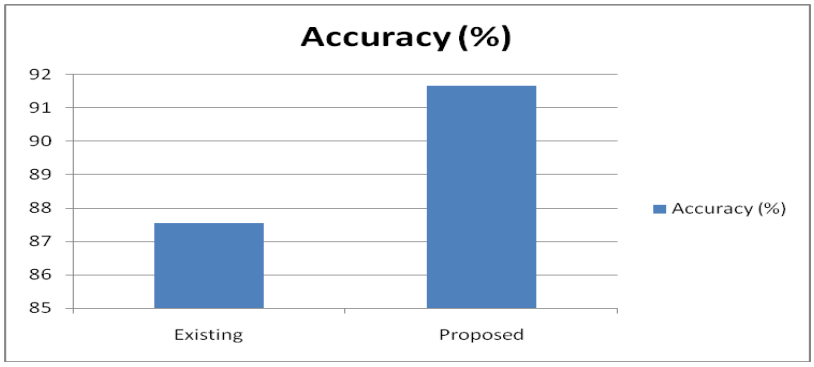

Fig.7. comparison accuracy level of existing and proposed

The fig.7. explain the accuracy level of 4:2 compressed multiplier technique is 87.55% and our propose 8:4 multiplier produced 91.67%

V.CONCLUSION

In recent trends multipliers are fundamental building blocks in Microprocessor, Digital signal processor and Embedded systems. Multiplier is one of the energy-hungry digital blocks. So, by designing the multipliers using compressors reduces the partial products which in turn increases the speed and reduces the delay. And also the power consumption by the digital circuit is minimized.

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