Power Efficient Clock Pulsed D Flip Flop Using Transmission Gate

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Abstract:
The need for low-power sequential circuits is pushing towards the implementation of low power consuming basic memory elements like D Flip-Flop. To accomplish power efficient D Flip-Flop, 180 nm CMOS technology is utilized to develop a novel eminent performance Current-Mode Pulse Triggered D Flip-Flop. Instead of voltage utilization in clock distribution is the new idea in the developed method uses current to render low power consumption clock signal. D Flip-Flop is designed by transmission gate which is also reduces the power consumption along with Current-Mode signaling. The Cadence - Virtuoso tool is to be used to simulate all the circuits with 180nm technology. Power consumption reduction in the designed D Flip-Flop is the foremost and major aim of the project. For reducing, power consumption in D Flip-Flop we are employing two methods. They are, Use of Current Mode Clock Distribution Networks (CM-CDN) instead of Voltage Mode Clock Distribution Networks (VM-CDN). Use of Transmission Gate Logic to implement the D Flip-Flop, instead of Static CMOS Logic.

Keywords: D-Flip-Flop, Current-mode, Virtuoso tool, transmission gate, CMOS logic

1. Introduction

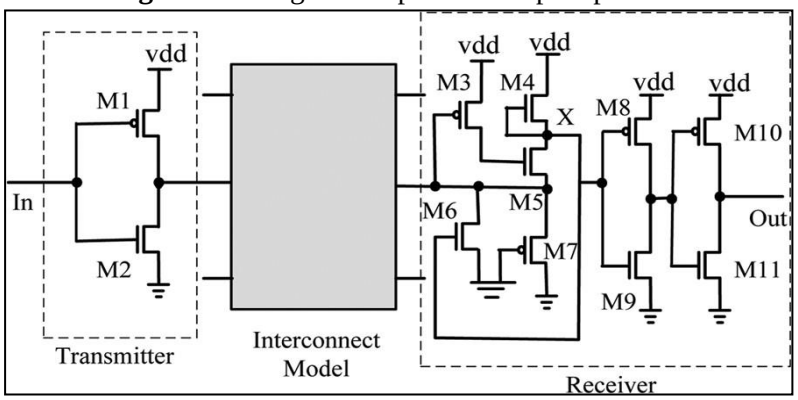
Our proposed idea completely revolves around key specification in the VLSI Design, which is power. The Power reduction in a VLSI circuit can be done in many possible ways. The main point to be considered while reducing the power is that it should not affect the other two specifications- Time and Area, in an adverse way. We consider the power reduction from the very starting point of the VLSI Design, which is the Clock Distribution Networks (CDN). Without being sufficed with one method of power reduction, using Transmission Gate Logic instead of Static CMOS has also been being used. Power is one the most important specifications generally spoke in VLSI Design. Area and Time are the other two specifications. All the three specifications have their own importance in their own way according to the field of application of the circuit/device. D flip flop is the most basic part of the circuits like shift registers, counters and many more synchronous and asynchronous circuits. It is the flip-flop which is most used because of simple implementation and easy input-output process. The power reduction in such a basic circuit element multiplies the effect i.e., the power in the circuits which use such type of flip-flops. This is another worldview for clock conveyance that utilizes current to circulate a clock signal worldwide as a substitution of voltage with diminished force utilization. Balanced signs are utilizing Current-Mode (CM) flagging. One-to-many clock conveyance organization is basically used the balanced signs. To attain the requirement, we make another elite Current-Mode Pulsed Flip-Flop with Enable (CMPFFE) **(Riadul Islam 2015).** The paper gives a profound knowledge to the plan of an adiabatic Johnson Counter which devours low force and conveys superior. For accomplishing low force dissemination in circuits the Complementary Pass Transistor Adiabatic Logic (CPAL) is utilized to plan the flip lemon. The plan of Johnson counter has been mimicked and confirmed. The Tanner EDA apparatus has been utilized to reenact every one of the circuits with 90nm innovation. Working inside the MHz recurrence band, the proposed configuration has shown lower power scattering **(Himanshi & Rajan 2015).**

2. Conventional Clocked D flip-flops

2.1 Voltage Mode-Clock D flip-flop

This is the traditionally existing and first model of D flip-flop. This model only focusses on the output rather than any of the three specification of the model efficiency. The voltage mode clock distribution networks are very widely used clock distribution networks in the real life applications. The schematic diagram of voltage mode pulsed D flip flop is shown in figure 1. This is due to the fact that it is easy to analyze and operate with the voltage sources rather that with current sources. On the other hand almost all the transistors and gates used are being designed on specifications provided with the terms involving voltages. The Voltage Mode Clock Distribution Networks beat D flip-flop is perhaps the most seasoned rendition of the D flip-flop. The force utilization of this sort of flip-flops is perceptibly high and the territory is low. At the point when executed as an individual circuit the time investigation was likewise demonstrated to be fulfilled. Be that as it may, the vast majority of the utilizations of the D flip-flop were found in the consecutive circuits like Registers, Counters and so on these sorts of circuits utilize various D flip-flops in arrangement to fulfill the necessary plan. At the point when the D flip-flops are utilized are in these circuits the force utilization is one of the significant issues which is to be considered. For meeting that determination numerous progressions are being made in the D flip-flop, till date. Regardless of the progressions made in the plan, the equivalent yet only the execution of D flip-flop is changes despite the working of the D flip-flop is consistent.

Figure.1 Voltage mode pulsed D flip-flop



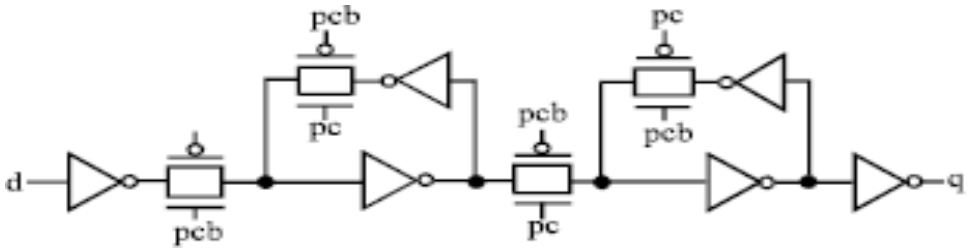
The voltage mode pulsed D flip flop has the advantages of easy implementation, area efficient and short delay and also it has the disadvantages are for sequential circuits this mode is not suitable. The voltage mode pulsed D flip flop is consuming more power and dissipated more power.

3. Proposed System

The existing system completely aims on reducing the power only by reducing the power consumed by the Clock Distribution Networks. By concentrating on the Clock Distribution Networks, it is true that the power consumption can be reduced to greater extent. There are also other methods of reducing the consumption of power by implementing the D flip-flop by more power efficient logic. One of such methods is implementing D flip-flop using Transmission Gate Logic (TGL).

Transmission Gate Logic is utilized to implement Flip-Flop register stage is the major idea of the proposed system. Leading-edge triggered D Flip-Flop with only clock signal without any Set, Reset and Clear signals is shown in figure. **d** denotes the input signal, clock signal is denoted as **pc , pcb** is the complement of the clock signal or it can be said as the inverted clock signal and D Flip-Flop output is denoted as **q** and it is shown in figure 2.

Figure.2 Proposed D Flip-Flop



In Flip-Flop the input is given at the **d** pin. Transmission Gates are provided with the mutually complement clock pulses. When the leading edge of clock pulse arrives, both the transistors, nmos and pmos of the TG-1 gets in to ON state and the input signal provided gets transmitted through the gate. Similarly the TG-2 which gets the clock pulses quite complement to the clock pulses received by the TG-1, and so the TG-2 remains in OFF state as neither of the transistors gets into active region. The TG-3 which receives the similar clock pulses like the TG-2 remains in OFF state for the same reason. Now the TG-4, which gets the clock pulses same as those of TG-1, gets into ON state and the data gets transmitted. Now since the data provided at the input doesn't get propagated to the output, the memory stage comes into the act. When leading-edge of the clock does not arrive D Flip- Flop has to maintain to the previous stage's output and it is done by the memory stage of the D Flip-Flop which is the salient feature of D flip-flop.

Figure.3 Final Structure of Proposed D flip-Flop

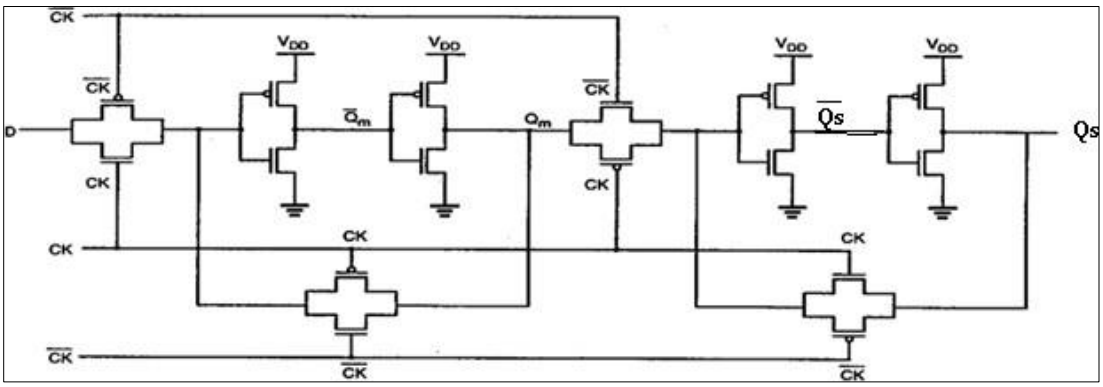
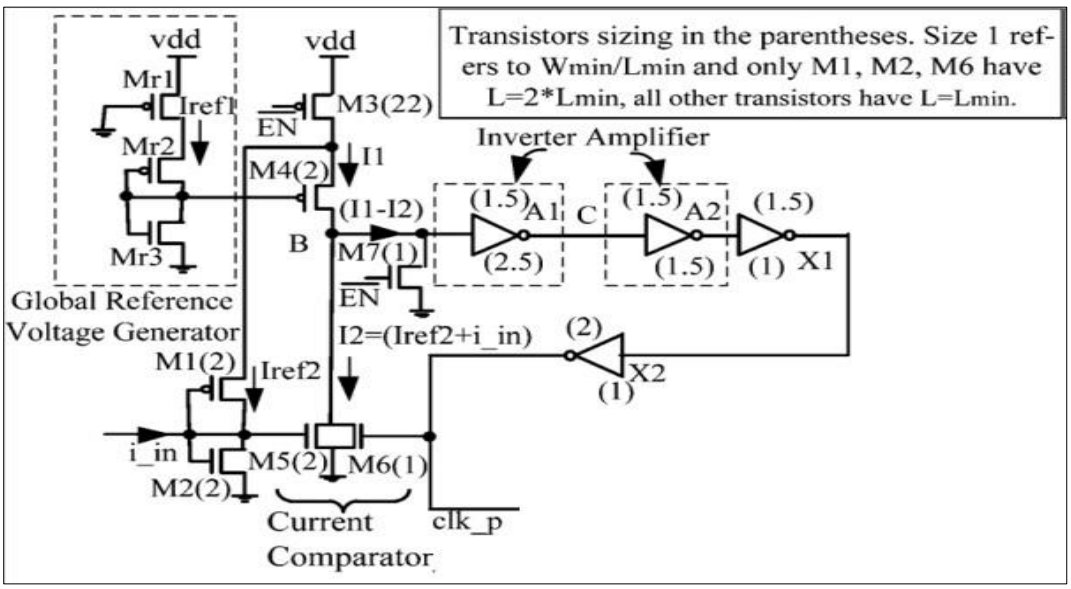


Figure.4 Current-Mode Clock Distribution Network



3.1 Design Considerations

In designing the nMOS switches, situated beneath the semiconductors, the channel source voltage of these switches should be considered since it may restrict the voltage headroom, limiting the upside of being utilized in low-voltage applications. To reduce this impact, low-resistance nMOS switches are required. At the end of the day, enormous semiconductors should be utilized. Since the parasitic capacitances of these switches don't influence the parasitic capacitances of the nMOS and pMOS semiconductors, it is feasible to ideally choose the size of the nMOS switch semiconductors such that both low-force and low-voltage activities are kept up.

3.1 Need for Transistor Sizing

MOS transistors are Uni-Polar Junction Transistors. The conduction in these transistors is due to the majority charge carriers only. In pMOS, the majority charge carriers are holes and electrons are the majority charge carriers in nMOS.The mobility of the electrons is approximately 3 times greater than that of the mobility of the holes. To improve the speed of the transistor, gate the width of the gate is increase which is known as transistor sizing. The transistor sizing is essential for equalizing the device pull-down and pull-up network's response time. The equation for the transistor sizing is given by the equation 1.
Generally,

$$\boldsymbol{W_p = 3 * W_n} \quad ----------(1)$$

Wp- pMOS transistor width and Wn- nMOS transistor width

4. Cadence Design Flow

Cadence Design System is an American Electronic Designs Automation (EDA) software and designing administrations organization, established in 1988 by the integration of ECAD and SDA Systems, Inc. The organization develops equipment and programming for planning incorporated printed circuit sheets, frameworks on chips (SoCs) and circuits. The supplier of designing administrations in the electronic plan mechanization (EDA) industry and electronic design technologies is Rhythm Design Systems, settled in San Jose, California. To help incorporate, confirm, and carry out complex computerized SoCs, there are arrangements that incorporate plan IP, timing investigation and signoff, administrations, and devices and techniques. The organization likewise furnishes items that help with the programming stages and advancement of complete equipment that help end applications. VIRTUOSO Platform - Tools for planning full-exceptionally coordinated circuits; incorporates schematic section, conduct demonstrating (Verilog-AMS), circuit reproduction, custom design, actual check, extraction and back-comment. This is utilized primarily for simple, inconsistent message, RF, and standard-cell plans, yet in addition memory and FPGA (Field Programmable Gate Array) plans.

Design streams are category into three different kinds. They are,

- Digital
- Analog
- Mixed signal

Digital Flow- Design utilizing a HDL.

- Synthesizer does (most) arrangement and enhancement of the plan.
- Designer may never at any point see the design.

- Requires standard cells upheld by the instrument - Flip-flops, inverter, cushions and so on

Analog Flow- It is schematic based plan stream and reenactment and manual arrangement and drawing, everything being equal. For the most part simple stream works with libraries from different devices.

Mixed Signal Flow- With both advanced (HDL) and simple planned segments in a solitary plan and it very well may be basically computerized and simple centered. The stream can be blend and match dependent on the plan.

5. Simulation Results

Before analyzing the average power consumed by the system, there is a need for Transient analysis of the same to ensure proper working and to calculate the average power. To calculate the average power in Cadence – Virtuoso, we use the Calculator option from tools in the Analog Design Environment (ADE) window. Other than Power, there are many more parameters like delay, which can also be found.

5.1. Conventional D Flip-Flop

The traditional D Flip-Flop, which has been discussed in previous section, that is VM CDN triggered static CMOS D Flip-Flop, have been subjected to *transient analysis* to make sure the circuit designed in the Cadence Virtuoso environment is working according to the logic, using 180nm technology. Once it is assured that the design is working properly, we can proceed to the analysis of the power using the calculator tool.

Figure.5 Schematic Diagram of conventional D flip flip

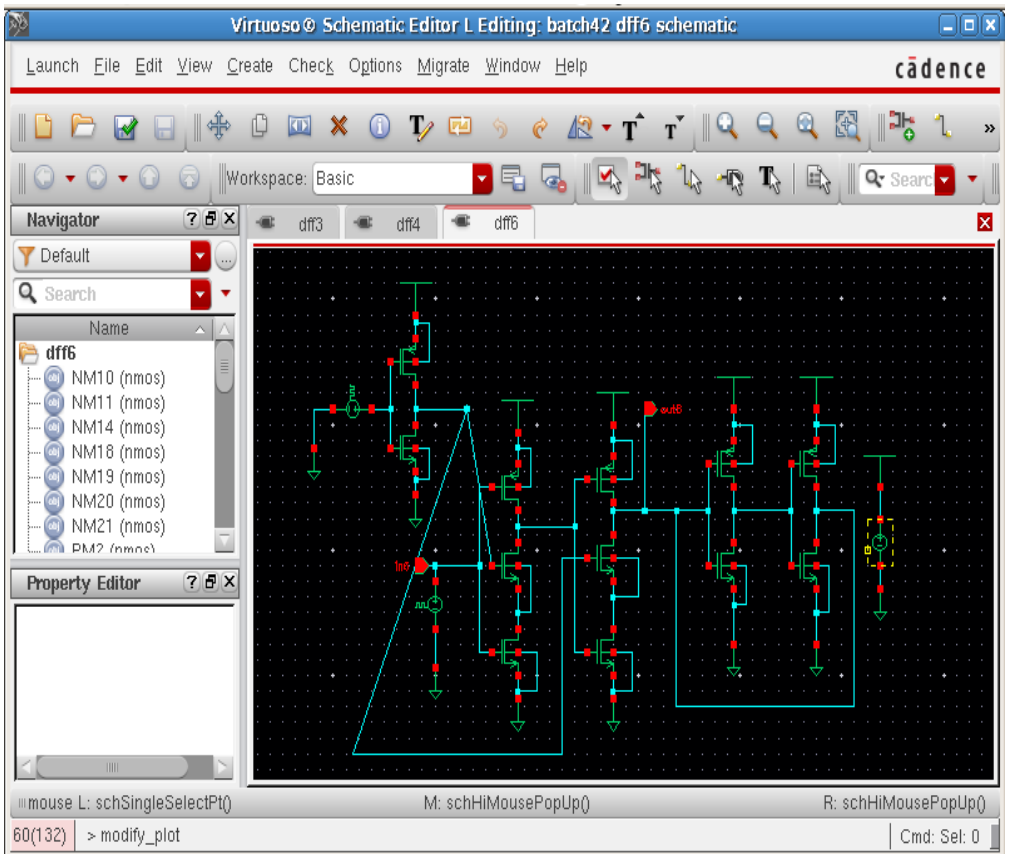
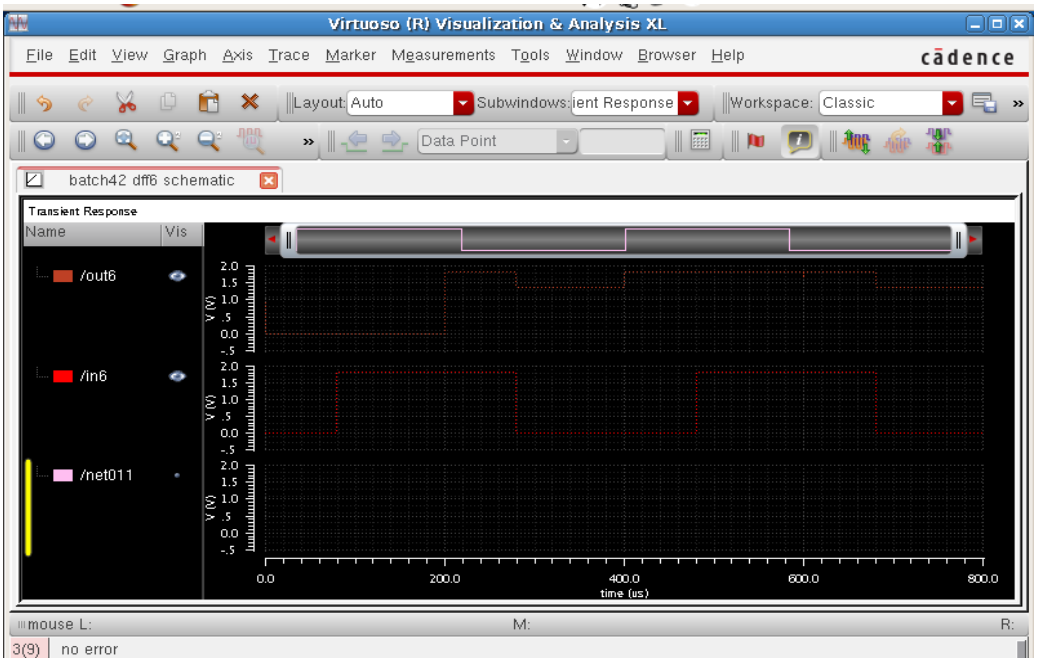


Figure.6 Transient analysis of conventional D flip flip



5.2. Existing System D Flip-Flop

Power analysis is carried out after the existing system D Flip-Flop Transient Analysis. D Flip-Flop output in transient analysis is required to find the average power consumed by the existing system. A lot has been discussed about the Existing model of the CM CDN D Flip-Flop in which D Flip-Flop implementation is utilizing Static CMOS logic. The average power and the instantaneous power are measured with the help of Flip-Flop output by utilizing calculator tool. We use Calculator from the Analog Design Environment (ADE) to find the various parameters like delay, power, and average power.

Figure.7 Schematic diagram of Existing CM-CDN Triggered D Flip-Flop

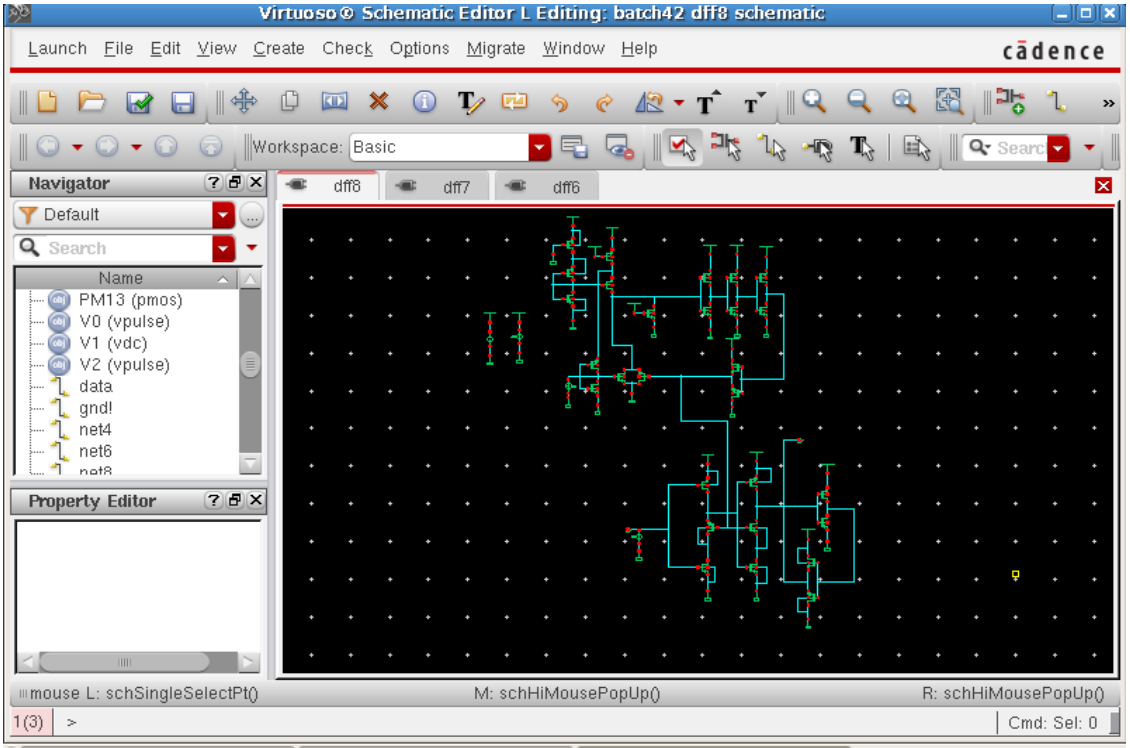


Figure.8 Global Reference Voltage Generator stage

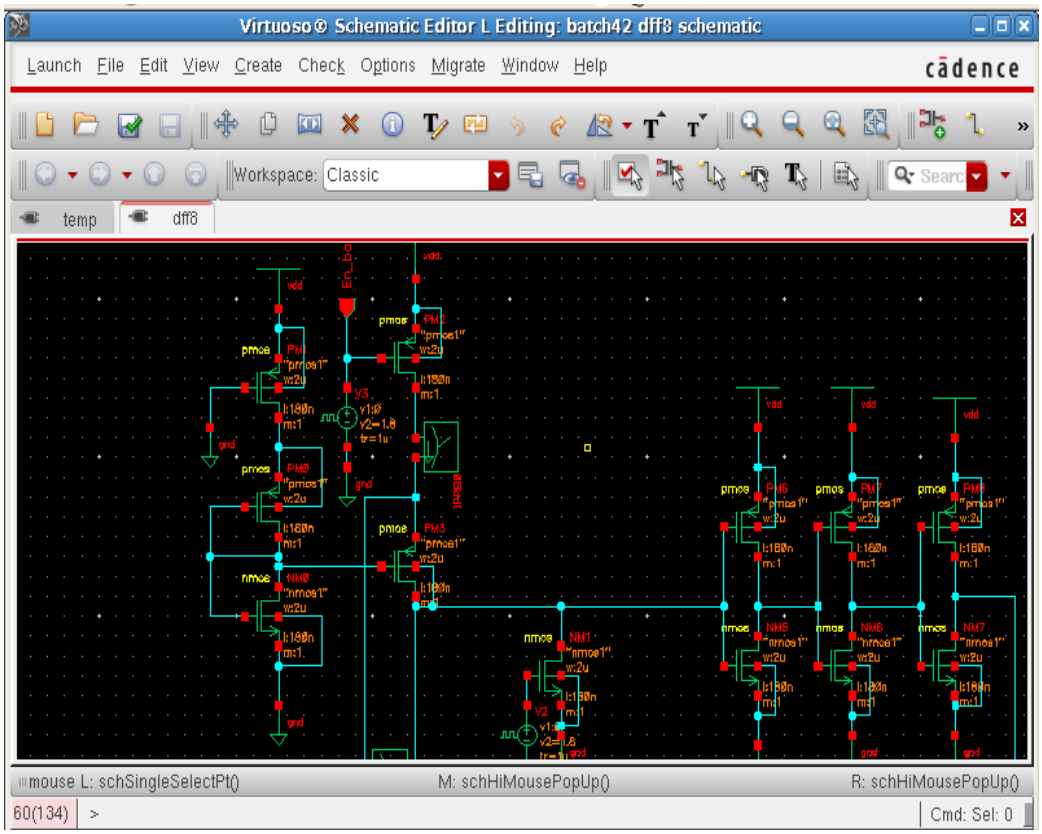


Figure.9 Inverter and Amplifier Stage

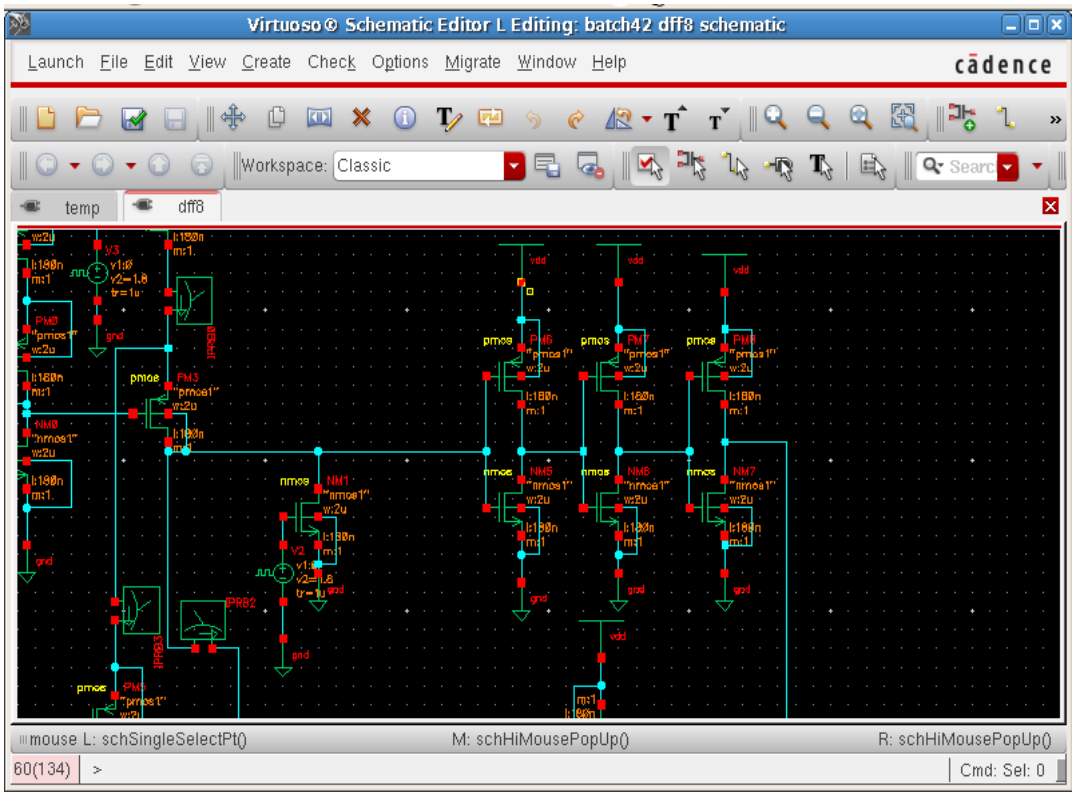


Figure.10 Register stage of the D Flip-Flop

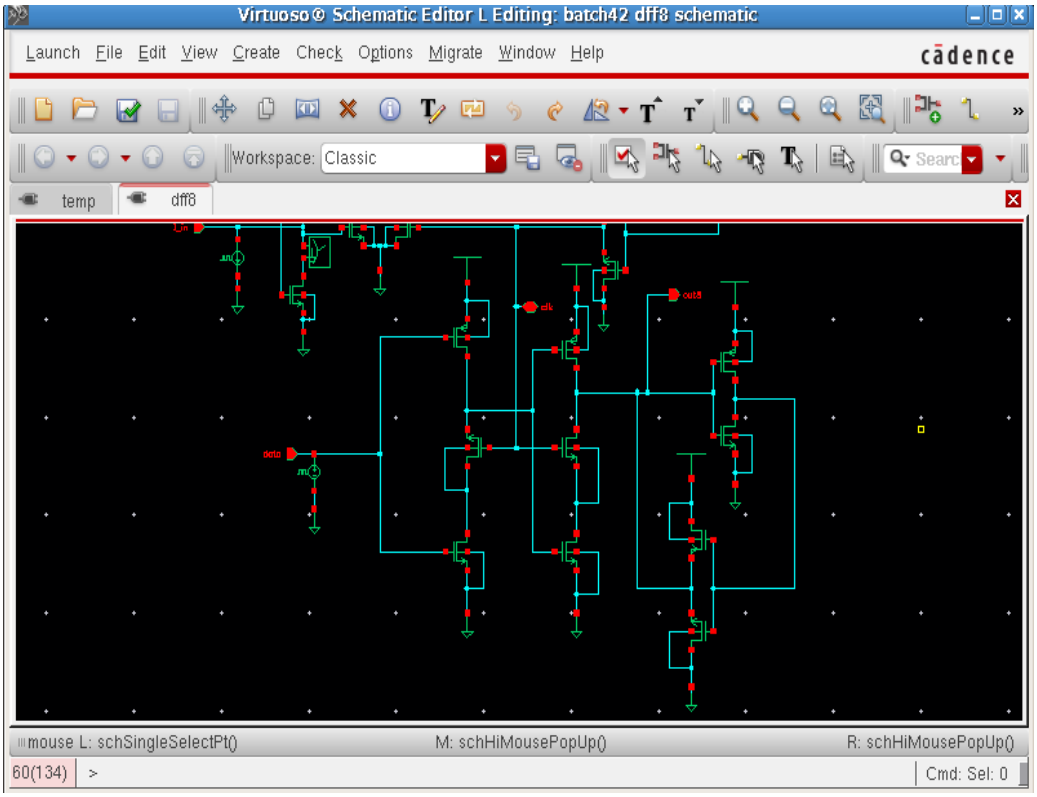


Figure.11 Current Input Stage

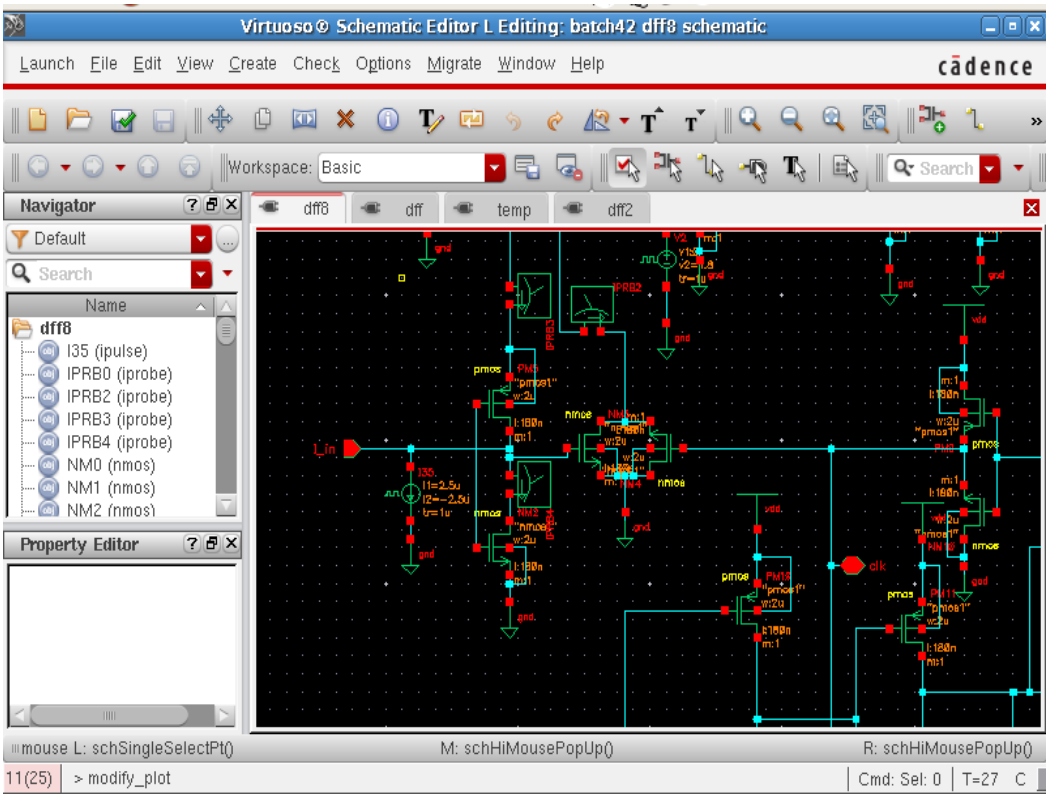
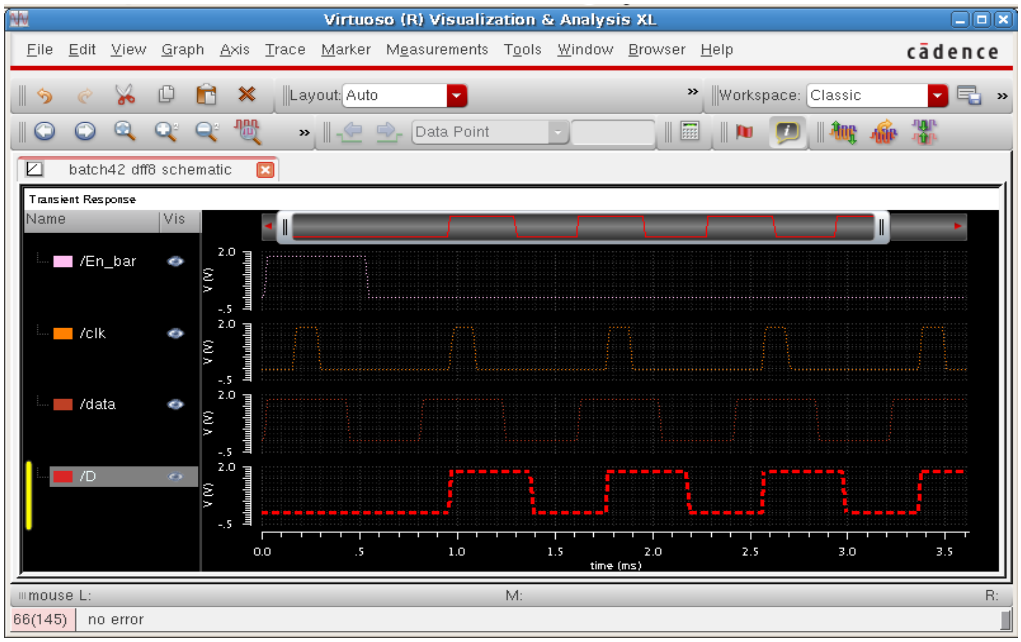


Figure.12 Output of the Existing System



5.3. Proposed System

This is the most anticipated part of this project. “The Proposed system”. For the proposed project completion, the proposed model D Flip-Flop Transient analysis plays a vital role. As it has already been discussed that the proposed model employs CM CDN instead of VM CDN and also it replaces Static CMOS logic with Transmission Gate logic. Similarly, the above two systems, the transient analysis is followed by the measurement of average power. Before measuring the average power, many times it is traditional to find out what is going on with the instantaneous power at several instants of time alongside the transient analysis. After measuring the instantaneous power, we proceed on to the measurement of the average power.

Figure.13 Schematic diagram for proposed system

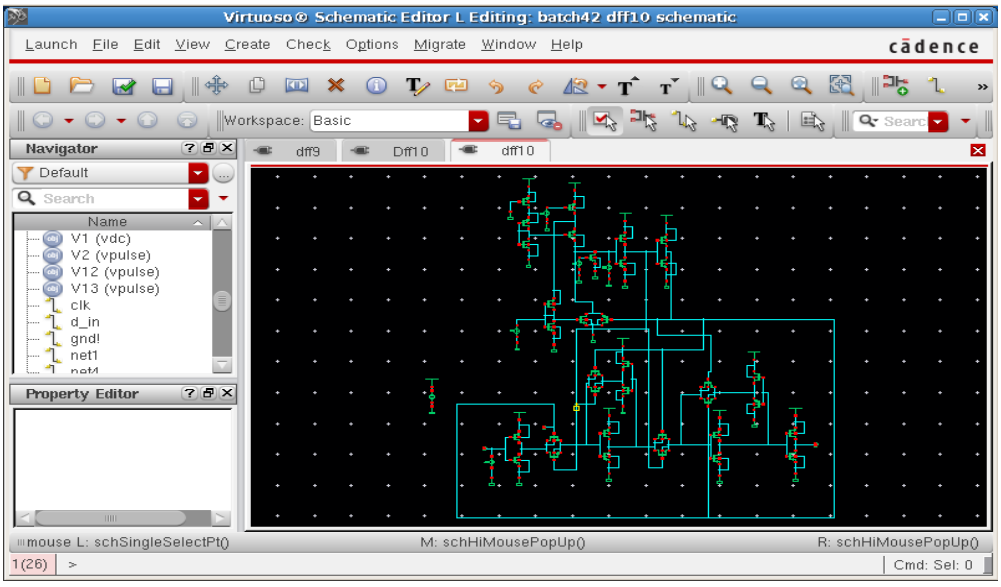


Figure.14 Flip-Flop's CM-CDN stage

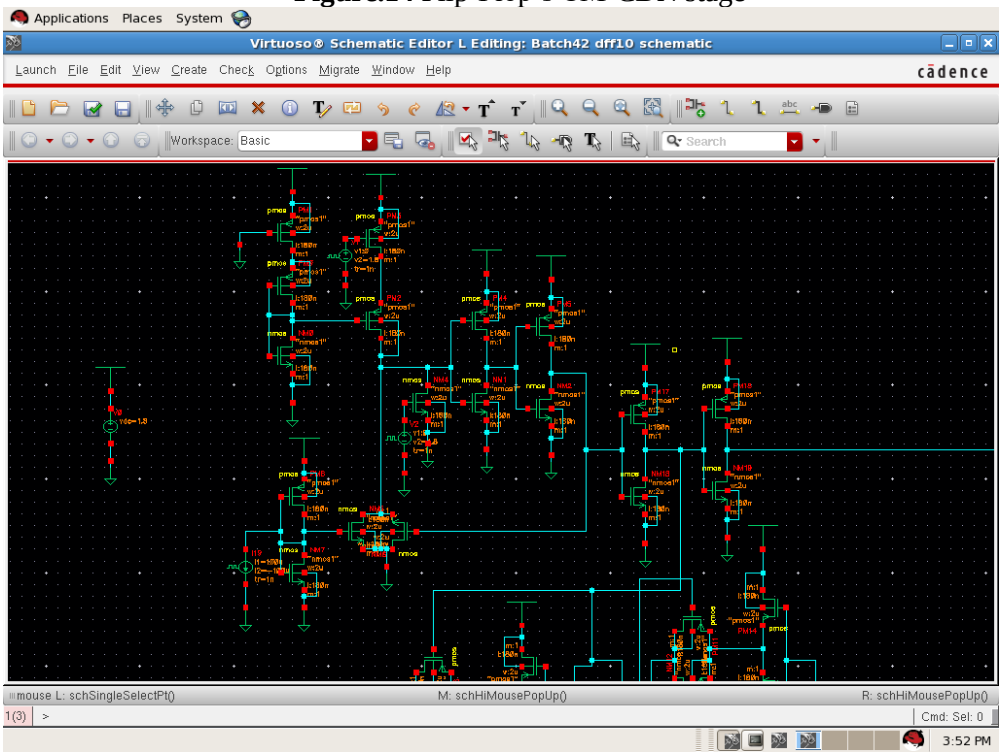


Figure.15 Flip-Flop's Register Stage

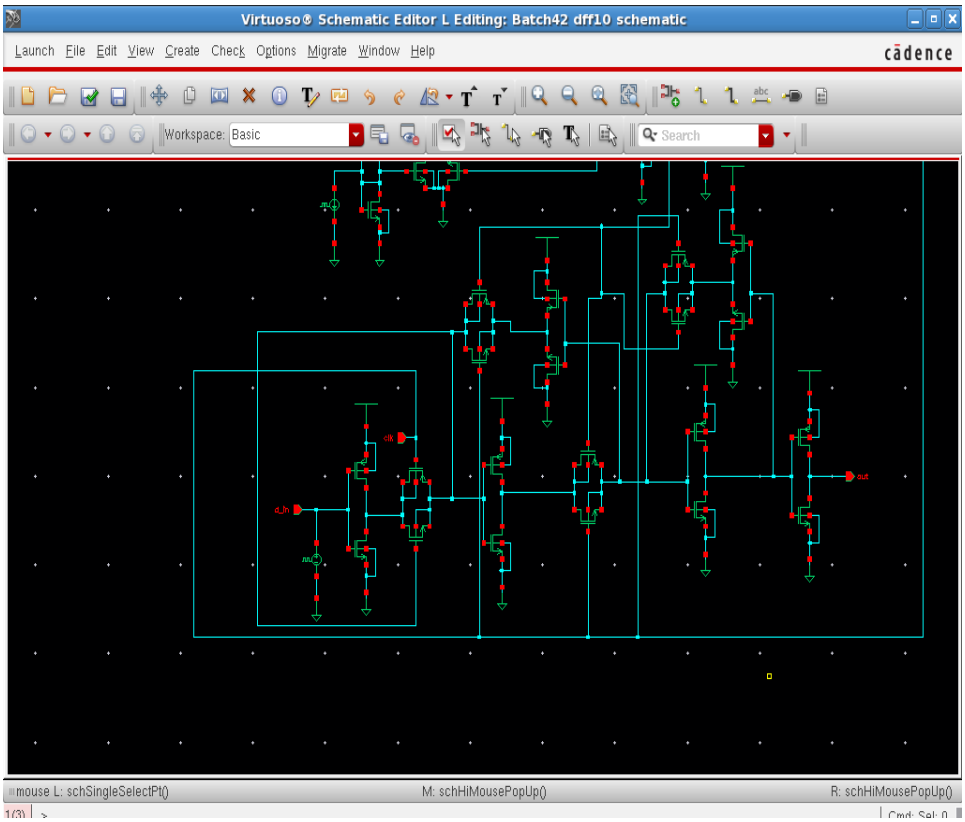


Figure.16 Output of the proposed system

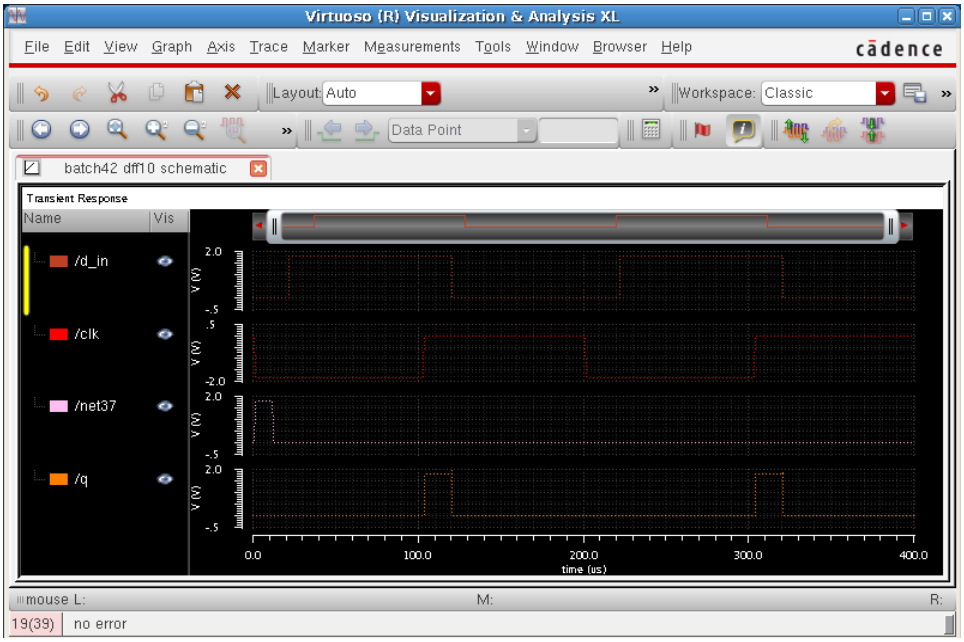
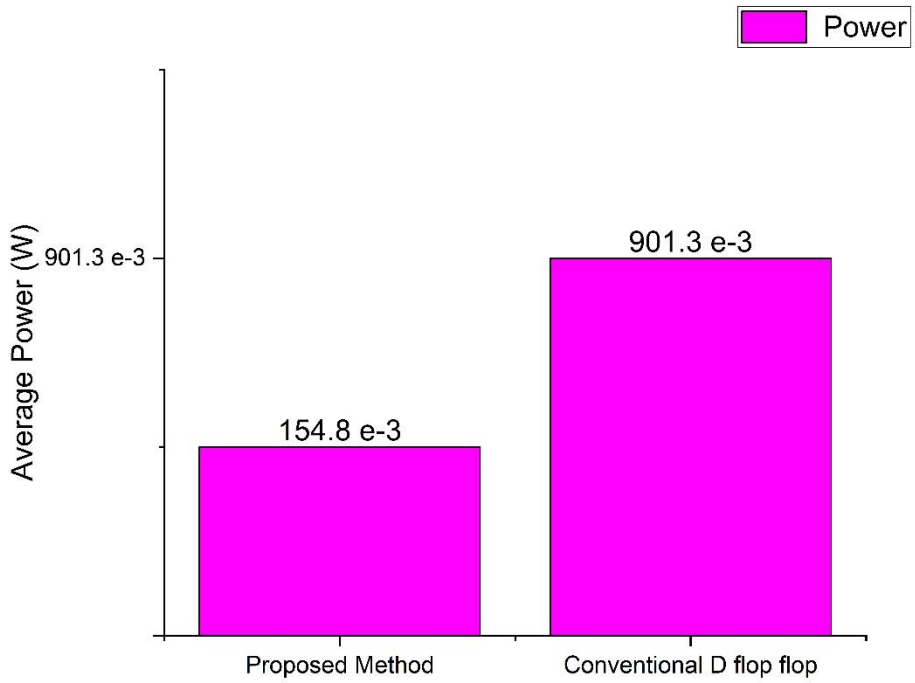


Figure.17 Average Power consumption analysis of proposed model with conventional model



8. Conclusion

The basic element of the proposed system is D Flip-Flop therefore almost all the synchronous and asynchronous sequential circuits, the reduction in power consumption in such a basic circuit element multiplies the effect as the size and complexity of the circuit, involving such type of D Flip- Flop, increases. The average power consumption in the Existing System in 180nm technology has been found to be **901.3e-3 W**. Whereas, the average power consumption in the proposed idea has been found to be **154.8e-3 W** is the proposed system average power consumption. Hence, from the result it is concluded

that proposed system average energy consumption is only **17.175%** of the existing system. Such a power efficient D Flip-Flop can be applied to low- power sequential circuits in the near future.

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