Research Article

Performance Analysis of Sepic Fed LCLC Resonant Converter for EV Battery Charger

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Abstract: EV'sare becoming more popular due to their eco-friendly nature. The existing topology of off board chargers are powered using a domestic meter. This results in high harmonic currents and hence, the domestic appliances get collapsed. Thus, to overcome this problem, this work proposes a novel charger unit which maintains power factor at unity. Thus, it contains two stages namely, DC-DC converter (SEPIC) at the first stage and 4 element resonant converter at the second stage. From the result, it is observed that the proposed changer exhibits better performance with low THD.

Keywords: SEPIC converter, Resonant converter(RC), FLC.

1. Introduction

The toxic emissions produced by automobiles have raised air pollution. Hence, to avoid usage of automobiles, EVwas introduced. However, the capacitance based battery for EV results in higher harmonic current. Thus, to eliminate the effects of harmonics in a power system, power factor corrector (PFC) converters were introduced.These convertors will result in reduced harmonics which in turn enhances the PF of the system.Among the PFC topology, to traditional boost converter plays a major role. Other than that, converter topologies like interleaved converter, bridgeless boost converter etc., were also implemented.But these topologies are subjected to various problems like inrush current, high ripples etc.

Apart from this, the dc link voltage produced by these converters is very low when compared tomaximum AC working voltage. So isolated transformers are utilized at the secondary stage of the converter. Hence resonant power conversion is utilized because it exhibits high efficiency and low EMI interference.Among the various topology ofRC, 3 elements topologies are widely implemented for power condition. However, it exhibits poor load regulation, at loading condition. Hence, to achieve better load regulation, this work proposed4 element topology.Thus, in this work a design of 4 element RC topology with SEPIC converter is attempted.

2. Material &Method

Thus, the block diagram representation of the proposed system is depicted in figure1.

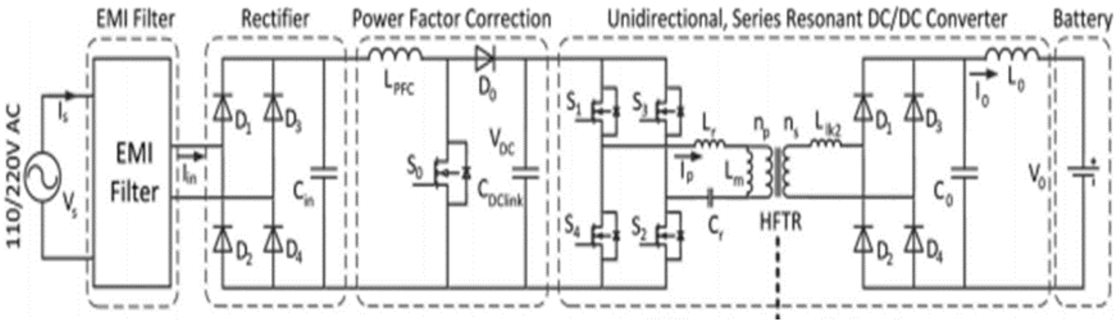


Figure 1. Overall Block diagram of proposed topology

It comprises SEPIC converter and four element LCLC topology to provide improved power quality operation over EV application.

Design of SEPIC converter

The SEPIC converter utilised in this proposed topology in depicted in fig 2 and waveforms of CCM mode is displayed in fig3

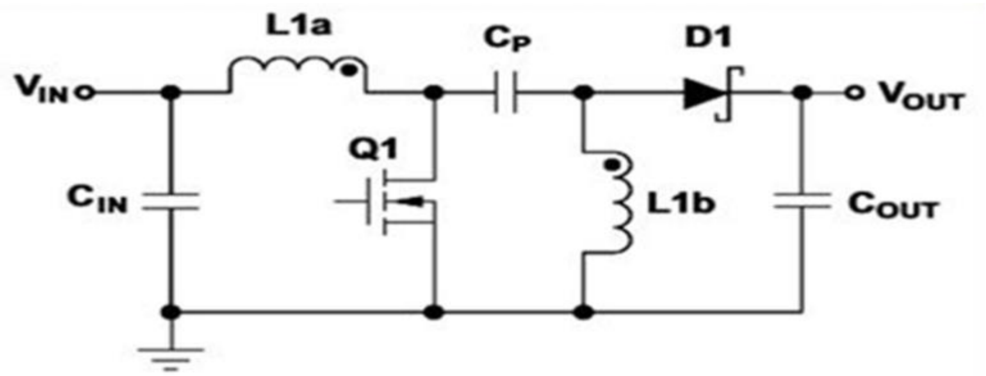


Figure 2. SEPIC Converter

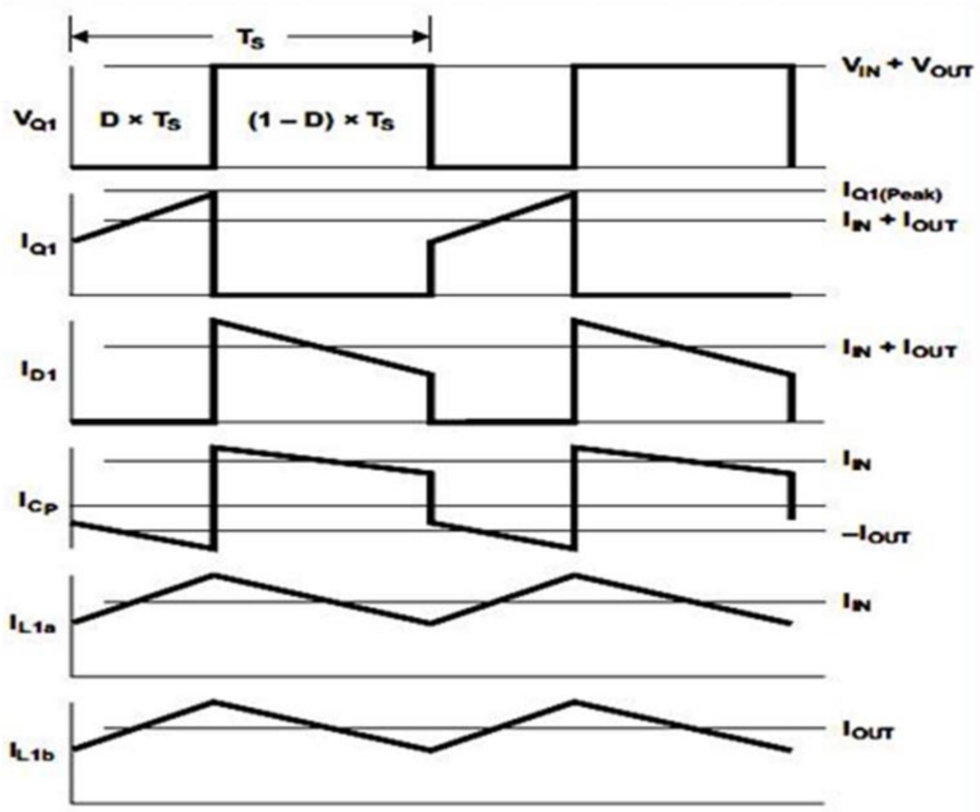


Figure 3. Waveforms during CCM operation

Thus the voltage gain of the SEPIC converter is formulated as

$$\frac{V_{out}}{V_{in}} = \frac{D}{1-D}$$

Design of LCLC converter

The schematic representation of proposed LCLC converter is depicted in fig.4.

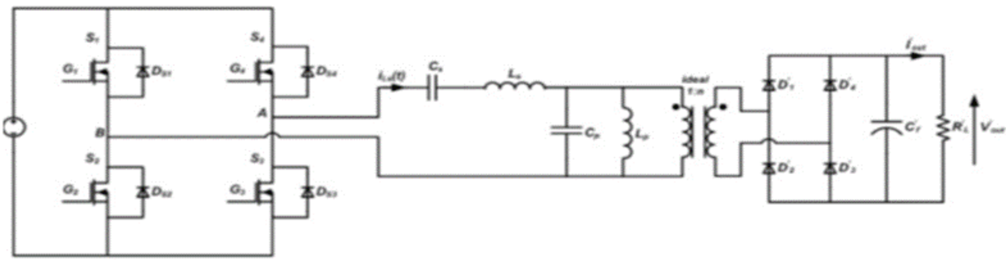


Figure 4. Schematic representation of LCLC converter

It comprises LCLC circuit, a transformer with higher frequency and a diode rectifier at its output. Thus, the waveforms of LCLC topology is shown in fig 5.

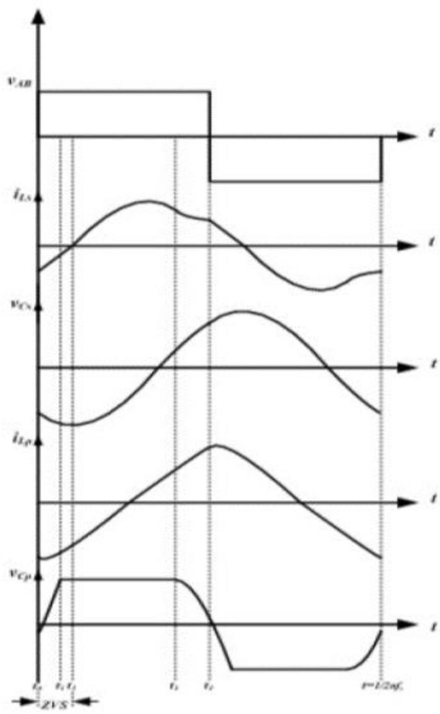


Figure 5.waveforms of the LCLC RC .

Design of fuzzy controller

Thus the proposed FLC is written off as follows

- Input and output variables are modelled using 7 fuzzy sets.
- Triangular MF is employed.
- Centroid method is adopted for Defuzzification process.

Thus, the MF e, ce and Δd are depicted in figure 6.

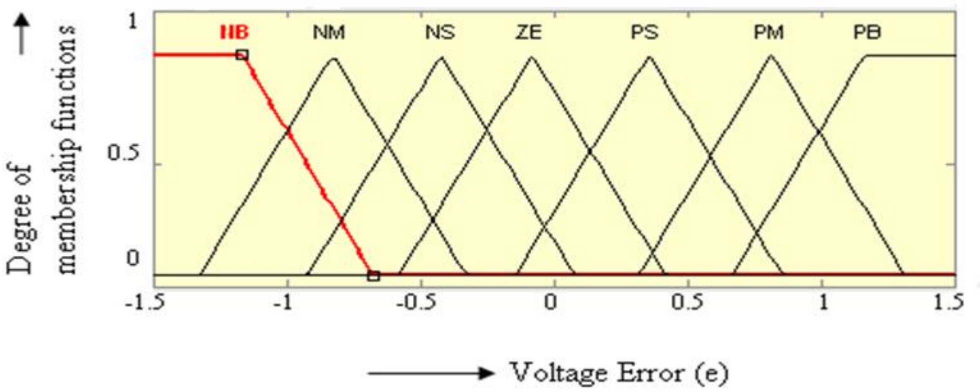


Figure 6a MF (e)

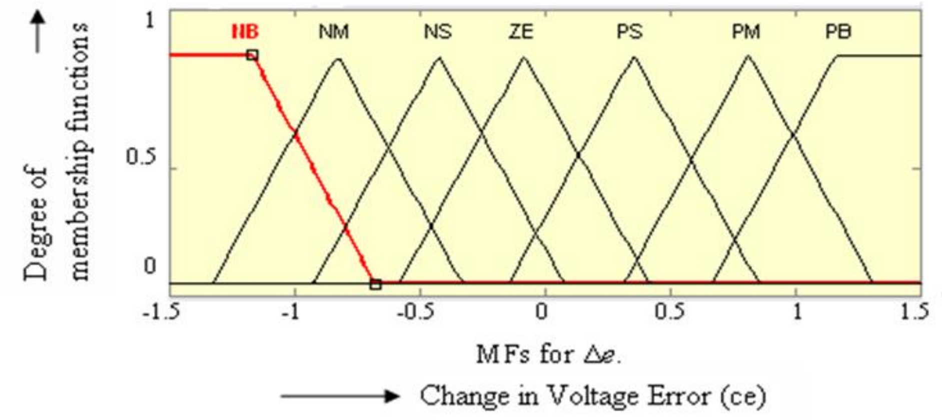


Figure 6bMF (□e)

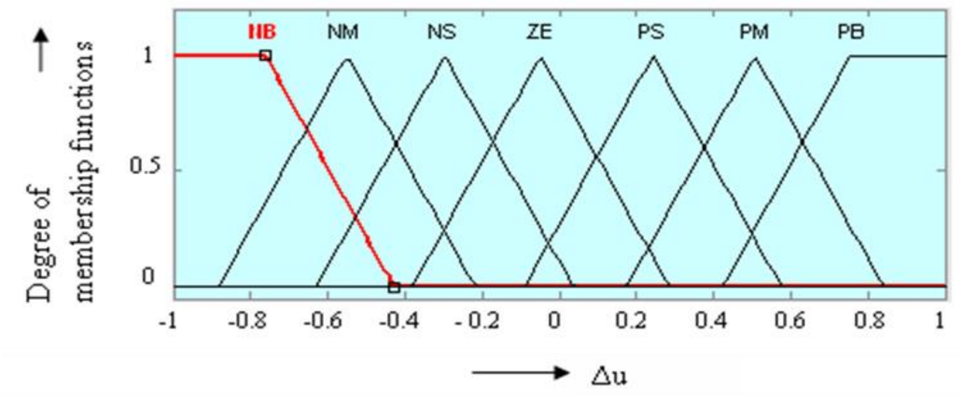


Figure 6bMF (Output)

3. Results And Discussion

A closed loop response ofproposed SEPIC based RC converter with FLC controller as described as follows. Fig. 7.1 to 7.6 displays the start-up / transients of the proposed topology with FLC controller under step disturbances in both load and supply.

The system is operated at fs about 100 KHz with operating voltage of 60V.

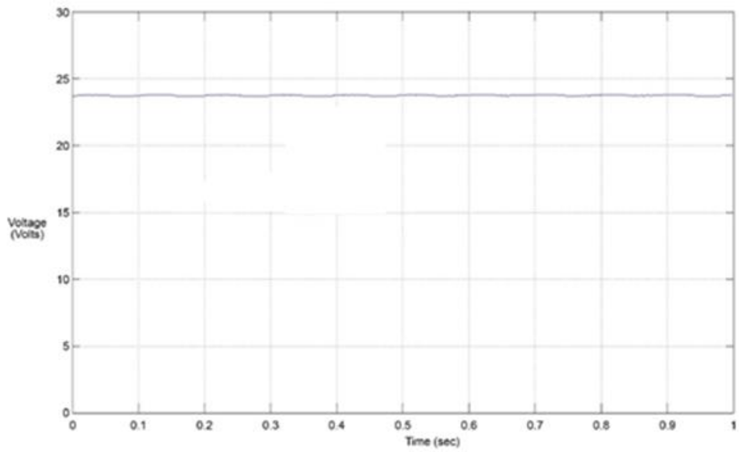


Figure 7.1 Output voltage of SEPIC converter

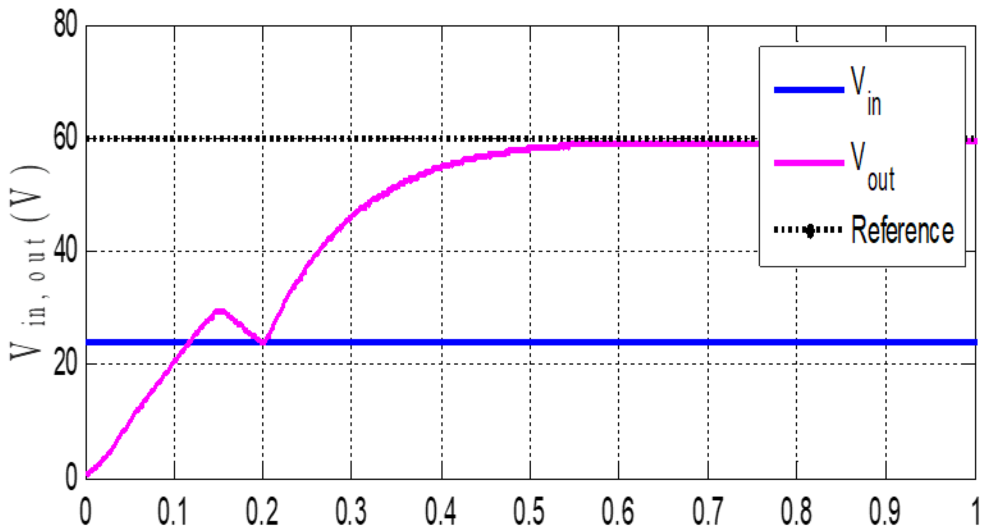
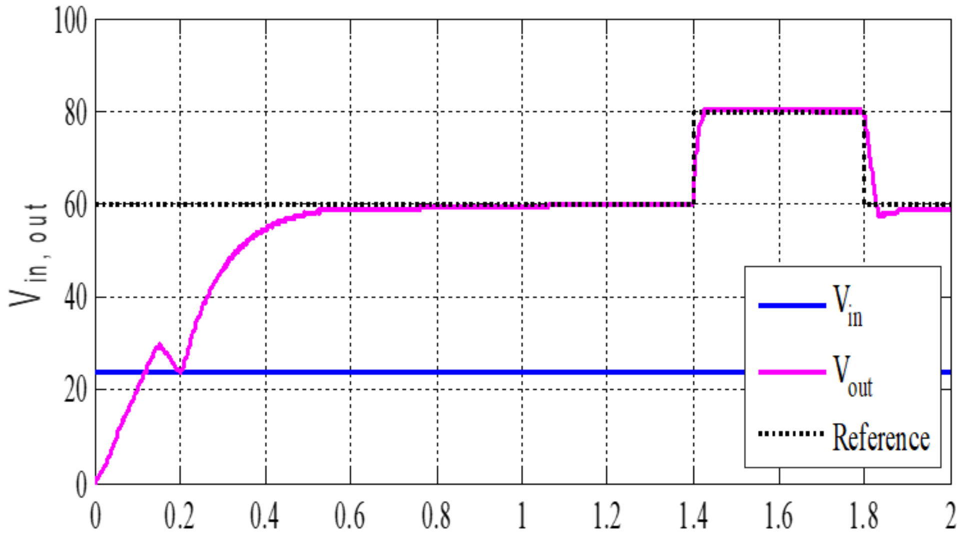


Figure 7.2 Voltage response of proposed topology

V=60V



Time in sec

Figure 7.3 Voltage response of projected system under different input conditions

(For, t=0 to1.4 sec, V= 60 V, for t=1.4 to1.8 sec, V=80V &for t=1.8 to 2.0 sec, V=60V)

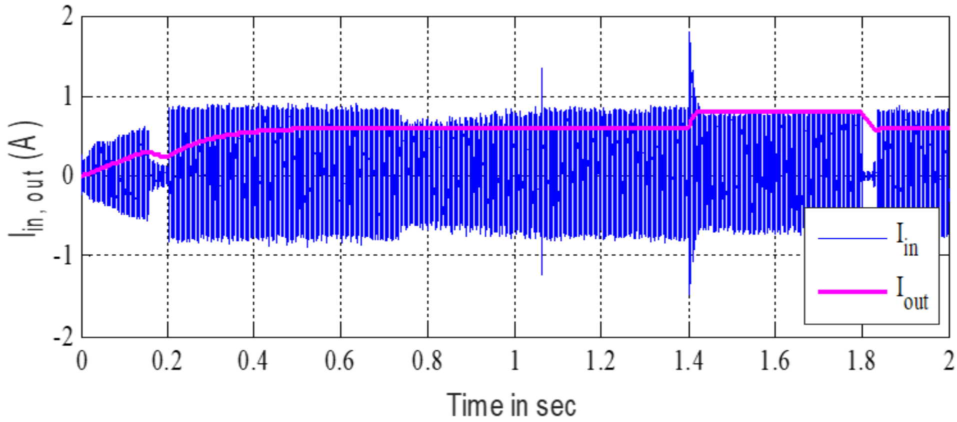


Figure 7.4 Current response

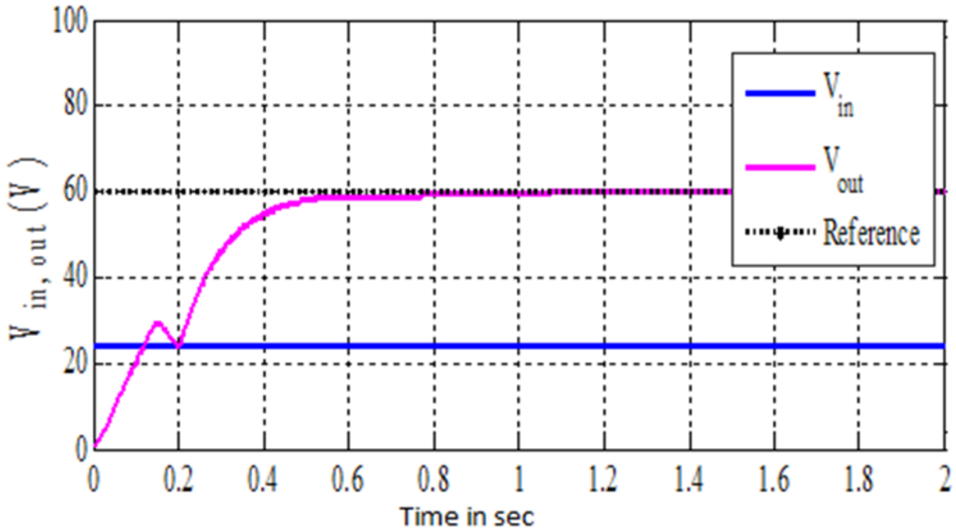


Figure 7.5 Voltage responsesunder load disturbances

(For, t=0 to 1.4 sec , R=100 Ω t, , t=1.4 to 1.8 sec, R=200 Ω , t=1.8 to 2.0 sec, R=100 Ω)

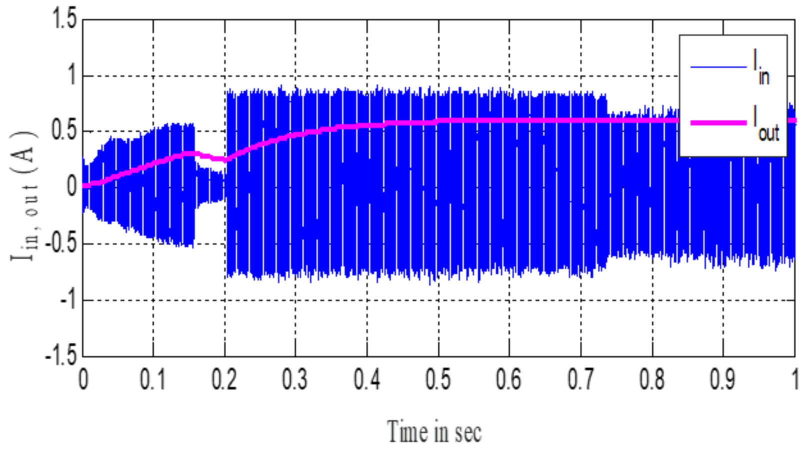


Figure 7.6 Current responseunder load disturbances

Figure 7.1 depicts the output voltage of the SEPIC converter. This voltage is fed as a input to the LCLC RC.The effect of voltage / Current variation based on input and load disturbances are depicted in figure 7.2 to 7.6.Thus, the from the analysis, it is noted that both changes in inputs and load has no effect over the proposed topology. Hence, it is more suitable for EV applications.

Thus, the performance of the proposed FLC in this topology is examined in terms of tr ,tsand is tabulated in table1.

Table 6. Performance assessment of FLC)

	Nominal Case			**Servo Response (Input)**				**Regulatory Response (Load)**			
				increase in supply voltage		decrease in supply voltage		Load Increased		Load Decreased	
Controller	**Ts (sec)**	**Tp (sec)**	**Ts (sec)**	**PO(%)**	**Ts (sec)**	**Under shoot (%)**	**Ts (sec)**	**Over shoot (%)**	**Ts (sec) (sec)**	**Under shoot (%)**	**Ts (sec) (sec)**
PI	0.53	0.9443	0.70	1.9	0.21	3.78	0.17	No change			
FLC	0.46	0.64	0.55	0.7	0.13	3.22	0.09	No change			

4. Conclusion

Thus, an enhanced power quality charger for EV is proposed in this topology. It comprises SEPIC converter along with LCLC RC. From the result, if is observed that the proposed FLC controller controls the system effectively even under supply/load changes. Hence, it is considered as a suitable charger for EV applications.

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