Design and Implementation of Low-Power Dynamic Comparator

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Abstract: Dynamic comparators are highly utilized in design of high-speed digital circuits. More precisely, Low power and high-speed dynamic comparators are the key elements in manufacturing of CPUs in many electronic devices. These CPUs consist of many comparison circuits known as comparators. This journal paper presents a low voltage thereby a low power Double Tail Dynamic Comparator (DTDC) with relatively less power consumption when compared to existing designs. In this journal paper, various types of dynamic comparators are discussed and compared with the proposed design. Dynamic comparators based on Double Tail technique, floating inverter amplifier technique and regenerative latch technique etc., are compared to the proposed design. This design is simulated using 250nm technology with the aid of Tanner EDA simulation tool. The pre-amplification process in this proposed design is implemented using Self-biasing technique. Self-biasing technique produces low kick back noise during the operation of this proposed design. The simulated results are mentioned below.

1. Introduction

In these days, Analog-Digital converters (ADCs) require high speed and more power efficient comparators. Because of this, design of high speed and low power comparators becomes more demanding in the CMOS manufacturing industry. Particularly, latch type dynamic comparator is preferred due to its high input impedance and very low static power consumption. [1]Today's modern comparators use dynamic pre-amplification process as the first stage in the comparison process. After pre-amplification stage, the output of pre-amplification stage is carried into regenerative stage.

At the earlier developing stage, single-stage dynamic comparators were designed. In single-stage dynamic comparators, a latch circuit is connected in series followed with a preamplifier circuit. But this design possessed a drawback. The kick-back noise which is produced by the means of capacitive path between output and input nodes. This kick-back noise is the reason why the single-stage dynamic comparators preferred as less power effective when compared to later develop more power efficient dynamic comparators. These dynamic comparators can be designed using energy efficient gates as mentioned in [1].

Dynamic comparators have developed in various types in due course of time. One of these types was strong arm latch type of comparators. These strong arm type latch comparators are more popularly used as regenerative comparators [2]. This strong arm type of comparator has less static power due to its strong positive feedback. This type comparator has only one stage design. Because of the one stage design, strong arm latch type comparators have large voltage headroom as mentioned in [3].

Two-stage dynamic comparators were introduced to get control of kick-back noise. Two stage dynamic comparator consists of two stages. The first stage in the two-stage dynamic comparator is called pre-amplifier stage[10-15]. The other stage of two-stage dynamic comparator is called latching stage. In the first stage, pre-amplifier circuit amplifies the given input signal. Pre-amplifier amplifies the given input signal to minimize the comparison time and therefore increase the comparison speed. The second stage, latching circuit is generally a circuit with inverters back to back[16-18] .The second stage carries out the comparison process in the two-stage dynamic comparator circuit.

2. Literature Survey

2.1 Conventional Comparator

Fig. 1 introduces the conventional two-stage dynamic comparator [3]. It comprises of a pre-amplifier stage and a latching stage. The low-tail current of the preamplifier stage is most preferred to minimize the input offset voltage. The latching stage is generally designed to produce a large operational current to increase the speed of operation.

When clock input is set to V_{dd}, transistors M7 and M8are in OFF condition. At the same time, transistors M1 and M2 are in ON condition. The nodes F_n and F_p will be discharging. During the comparison phase in this design, when clock input is set to low, transistors M1 and M2 are in OFF condition. At the same time, M7 and M8

are in ON condition. During this period of time, the paths F_n and F_p are charged to V_{dd}. Meanwhile this causes the output paths Out_p and Out_n to discharge through transistors M11 and M12 to the ground. [3]

This two-stage technique [3] has an advantage of resulting in low kick-back noise which is further useful for low-voltage applications [4]. This conventional dynamic comparator is simulated on 180nm CMOS technology using Mentor Graphics.

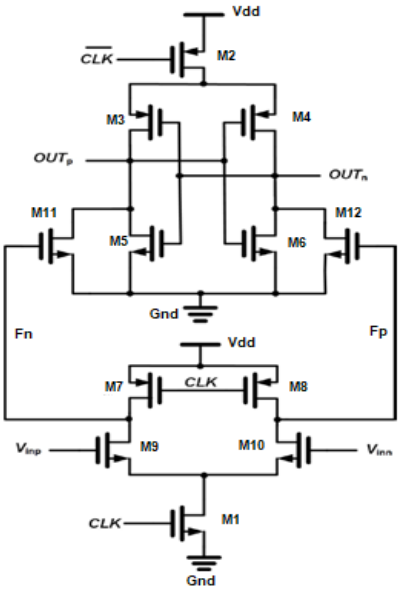

Figure 1. Conventional Dynamic Comparator

2.2. Dynamic Comparator

This paper [5] consists of a comparator design which reduce the power consumption of the circuit without the usage of any additional capacitors or complex design but with a cross coupled architecture in the input signal in the pre-amplifier stage. This design [5] is fabricated with a supply voltage of 1V. This design architecture prevents internal nodes of the dynamic comparator from discharging fully for small input signals and therefore reducing the power consumption for each comparison. This design [5] is fabricated using 65nm CMOS technology. This design is simulated using a supply voltage of 1.2V.

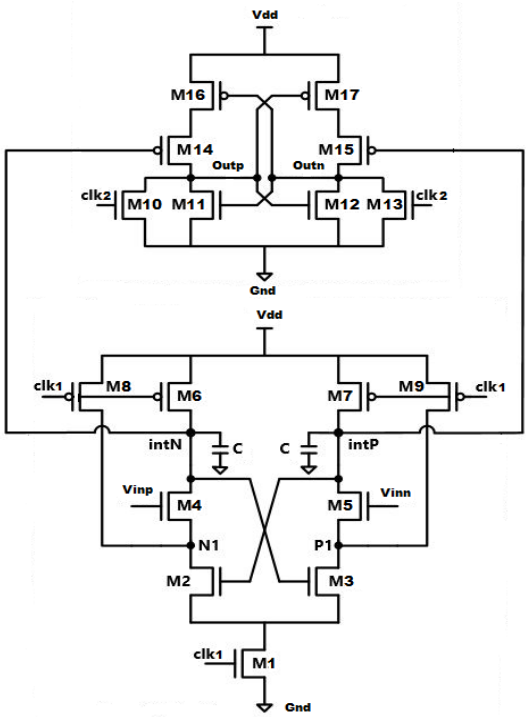

Figure 2. Dynamic Comparator

2.3 Floating Inverter Pre-Amplifier Based Dynamic Comparator

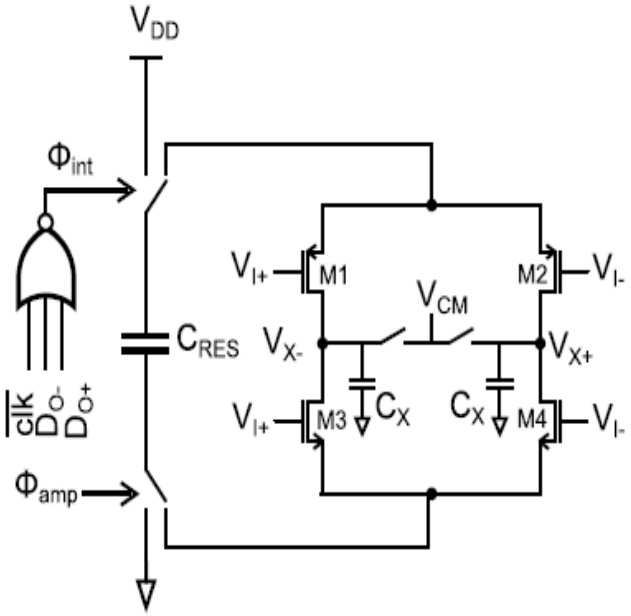

Figure 3. Floating Inverter Pre-Amplifier based Dynamic Comparator

In this design [6] , in order to improve the power efficiency of the pre-amplifier stage to some more extent, CMOS DB integration technique is used. This design i.e., CMOS DB integration, when combined with input signal powered by two tail capacitors, is shown in Fig.3. In this design [6], during the integration phase, the bottom source node *VS*− increases, while the upper one *VS*+ decreases.

In this design, during the integration phase, only the differential charge is integrated on the loading capacitors, and the common-mode voltage stays constant, which is 0.6 V if the given supply is 1.2-V. It prevents the full discharge of the capacitor *CX*. [2]

2.4 Regenerative Comparator

Regenerative comparators [7] produce high-efficient output by consuming low power when compared to existing designs. Comparators in which high gain amplifiers [7] are connected in series are not used nowadays in high-speed digital circuits which contain clock input [4] [8]. Instead of these circuits, regenerative circuits are small in size and has almost zero static power been widely used nowadays. In this paper [7] , design and analysis for regenerative comparators was presented.

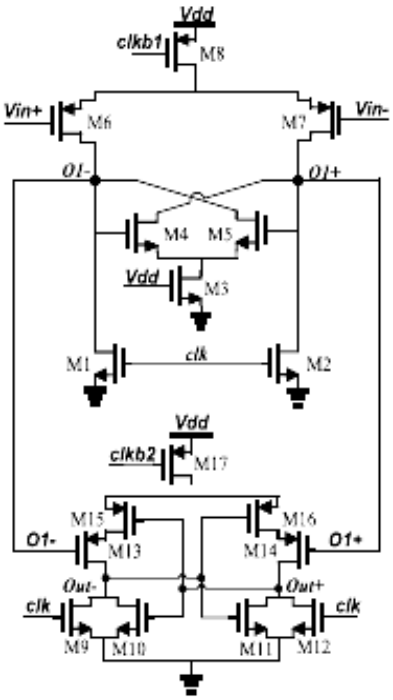

Figure 4. Conceptual Regenerative Dynamic Comparator

2.5 Low Power High Speed Comparator

The low power high speed comparator [9] is shown in Fig. 5. In this type of dynamic comparator, a pMOS latch is used in the latching stage. The proposed structure [2] can also be designed using nMOS technology, i.e., latching stage and preamplifier stage are designed using nMOS transistors. This design results in a high-speed output because nMOS transistors have high mobility than pMOS transistors. The size of M4, M5 transistors is adjusted to a large size to make the output common-mode voltage of the preamplifier as small as possible.

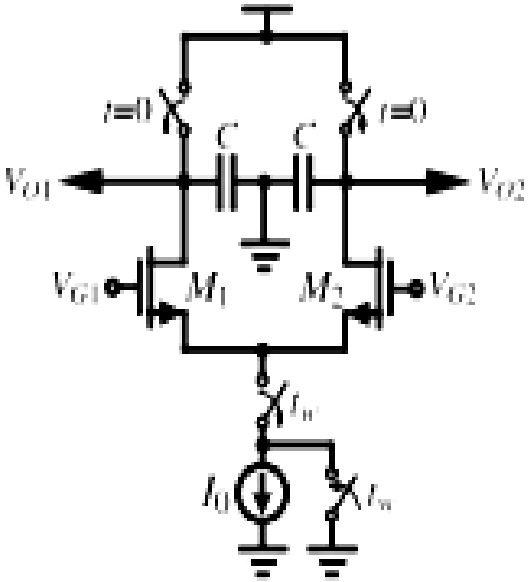

Figure 5. Low Power High Speed Dynamic Comparator

3. Proposed Design

Fig. 6 represents the schematic design of our proposed low power dynamic comparator with a modified latching technique.clk2 is the voltage level-translated signal of clk1 with 95 ps delay. These voltage level translators are used to translate signals from one voltage level to another which allows compatibility between circuits with different voltage requirements. In this dynamic comparator, when clk1 input is low, nodes F_n and F_p are set to V_{dd}. At this instance, transistors M11, M12, M5 and M6 are in ON condition, whereas M9 and M10 are in OFF condition. Nodes D_n and D_p are discharged to ground via transistors M5 and M6, and nodes Out_p and Out_n are set to V_{dd} via transistors M11 and M12.

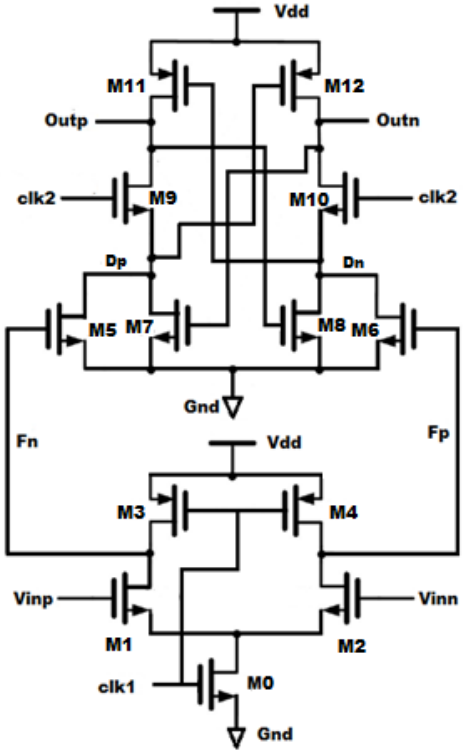

Figure 6. Proposed design of Low Power Dynamic Comparator.

There are numerous designs with cross coupled architecture. This proposed dynamic comparator is a type of cross coupled techniques. This proposed design is implemented using cross coupled inverters. Generally other cross-coupled techniques will bias only two transistors in the strong-inversion region. At the same time, other two transistors will be in the cut-off region. Strong inversion region means nothing but saturation region where drain-source voltage is less than or equal to the difference between gate-source voltage and threshold voltage. Cut-off region means the region in which there is no drain-source current flowing from drain to source in a MOSFET. In this cutoff region, the transistor behaves like an open switch i.e., the transistor will be in OFF condition. But in this proposed design, all the transistors M7, M8, M11 and M12 which are cross coupled, are biased in the strong-inversion region.

This design has two phases. One is pre-amplification phase and the other is comparison phase. This design is more power efficient than existing designs because the proposed technique has higher total trans-conductance than the other designs at the comparison phase. This parameter leads to the increase in speed of comparison among other designs. Whenever fast comparison speed is achieved, meta-stable period will be reduced. Therefore the power consumption is reduced up to a significant extent. In digital circuits, meta-stable condition occurs when two signals combined in such a way that their resulting output leads to an intermediate state i.e., the output is neither low nor high. Such situation is called meta-stable state.

4.Results and Discussions

While comparing the proposed and other dynamic comparators, the proposed design was simulated in 250nm CMOS technology with 1.2V supply voltage. This proposed Low Power Dynamic Comparator was simulated in Tanner S-Edit tool. This design was simulated using 250nm (0.25µm) CMOS technology. At first, schematic should be drawn on the S-Edit. Later add all the useful libraries to the schematic. Next, configure the parameters which should be measured in the "Setup" icon.

Then save the schematic. Click on "Run Simulation" button. Then T-Spice will be opened, and SPICE commands are executed as shown in the figure 5. After successful execution of T-Spice file, waveform will be opened in "Waveform Editor"application. To know the power consumption of the design, add a SPICE command ".power". The measured power consumption was mentioned below in the figure 8.

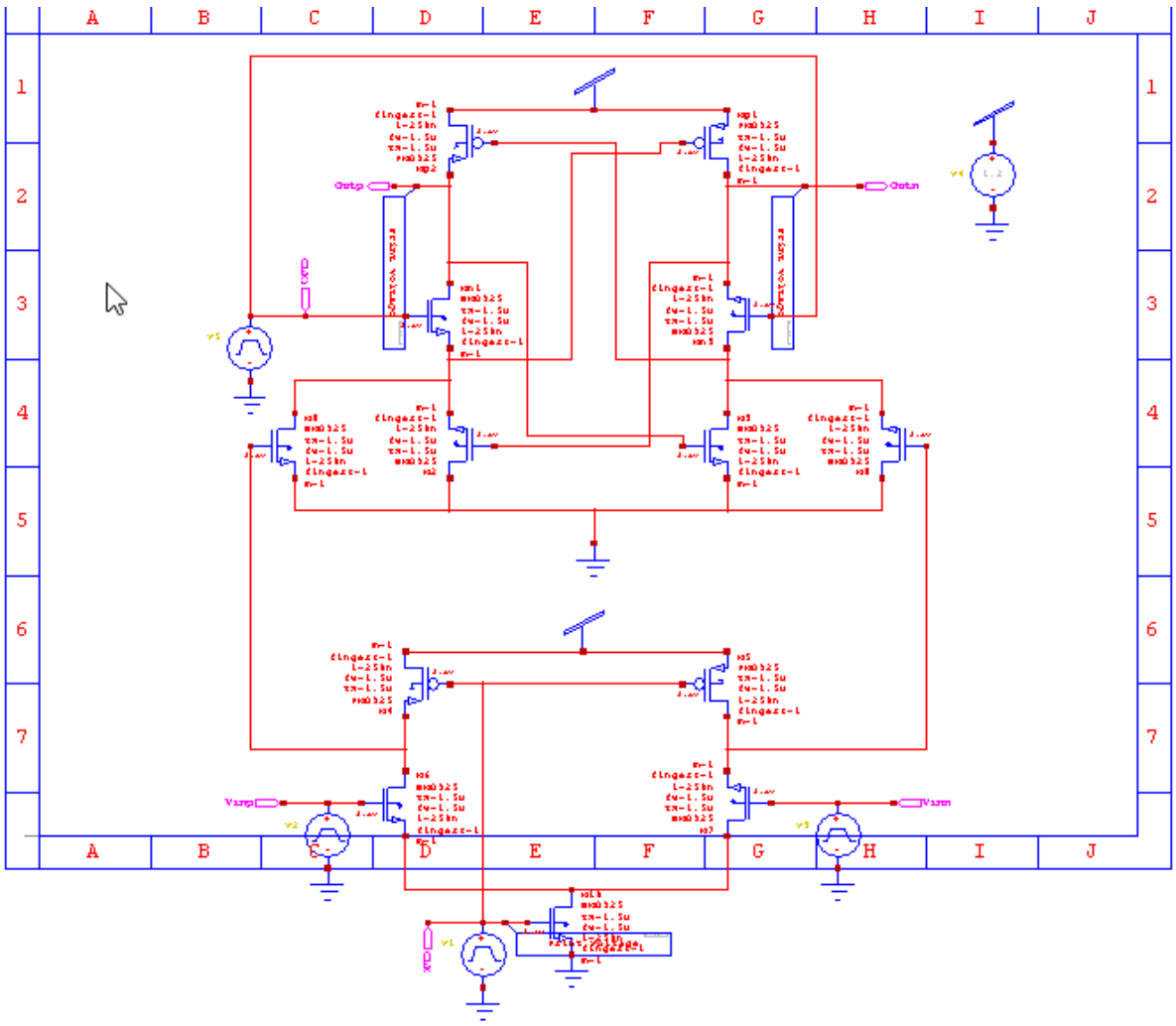

Figure 7. Picture depicting the Simulation of proposed dynamic comparator.

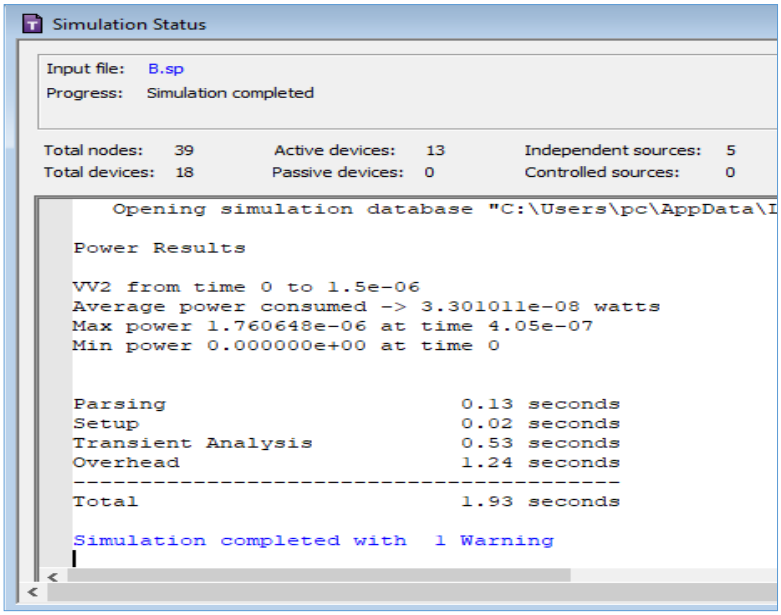

Figure 8. Power consumption

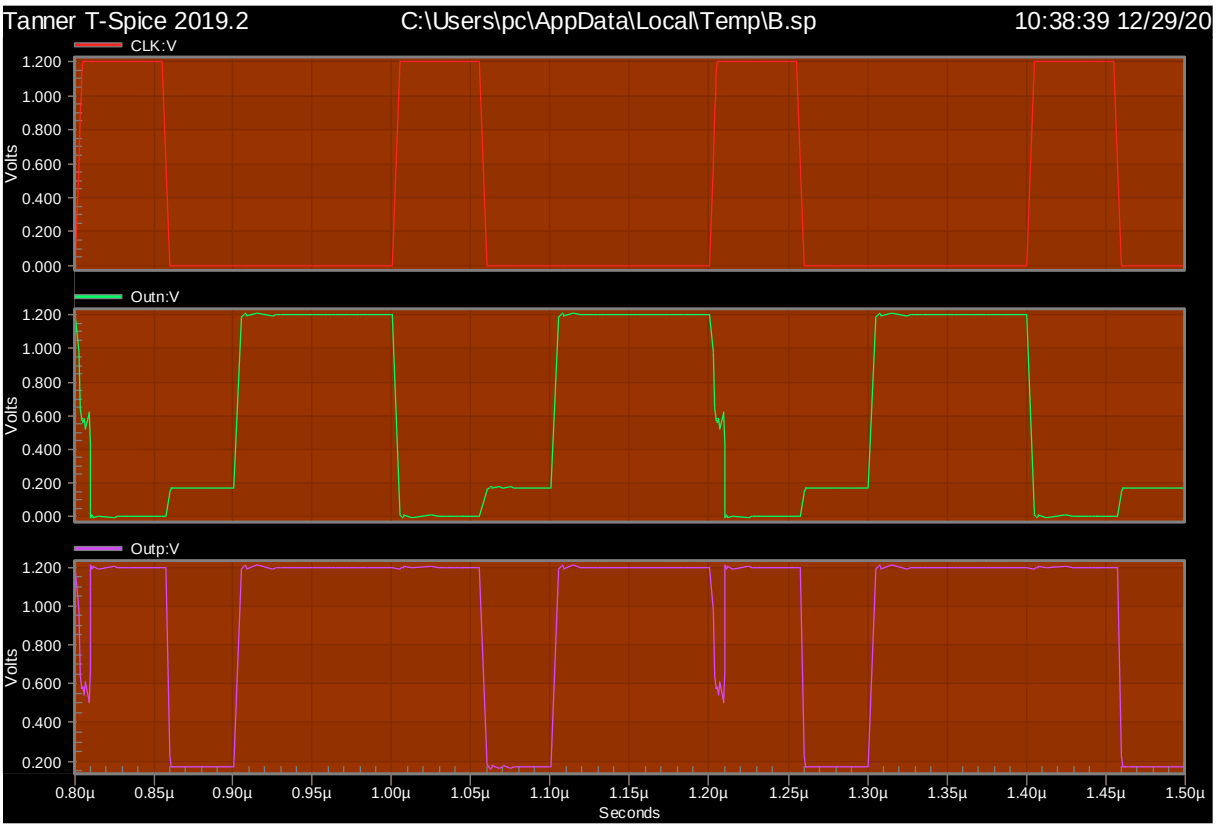

Figure 9. Waveform depicting Output

5. Conclusion

This journal paper presents a low voltage thereby a Low Power Dynamic Comparator with relatively less power consumption when compared to existing designs.This proposed Low Power Dynamic Comparator was simulated in Tanner S-Edit tool. This design was simulated using 250nm (0.25µm) CMOS technology.

The proposed dynamic comparator in this paper which includes a power efficient cross-coupled latching stage is not only suitable for low-power but also for high-speed applications. In this design, all cross-coupled transistors are biased in the strong-inversion region. The performed simulations results show that the existing

comparator designs are more power consuming. With the help of this proposed technique, power consumption is reduced to a greatest possible extent compared to those of the pre-existing dynamic comparator architectures.

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