Design of Area Efficient Low Power Ever Mixed Logic Line Decoders and Comparator

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Abstract: Mixed logic designs take a prioritized place in logic design approaches which will give a simplified mechanism for the analysis of digital circuits. The right utilization of mixed logic notation produces logic expressions and logic relations that are analogs of each other. Also, a mixed logic implementation gives clear idea with regards to the activity of a circuit. Here in this article, we introduced mixed logic designs like pass transistors (DVL), transmission gate (TGL), static CMOS. By using CMOS technology, it requires 20 transistors to design 2:4-line decoder but by using this mixed logic we can design the same 2:4-line decoder with the use of 14 transistors (14T) only. Furthermore, 4:16 line decoders are designed with this novel mixed logic topologies. Introducing mixed logic approach a 2-bit comparator was designed by using 4:16 line decoder mixed logic. All proposed circuits have a smaller number of transistors and designed by using novel topologies, these logics proves in reducing the transistors count, power, and delay in a satisfying level. Finally, a variety of simulations are carried using DSCH and MICROWIND tools at 7nm range to examine all notable changes in parameters.

Keywords: Logic gates, 2:4 CMOS line decoder, 4:16 CMOS line decoder, mixed logic design, 2-bit comparator

1. Introduction

CMOS technology was used in all circuits and integrated circuits. Static CMOS was preferred because of complementary pMOS network and nMOS networks which gives good results in performance as well as noise resistant and variation of device. Therefore, for robustness against sizing of transistor and voltage scaling [1]. For Reliable operations at small transistor size and small voltages CMOS logic was characterized.

We are here proposed various designs like pass transistor and transmission gate for the alternative of Static CMOS logic. Only applications of inputs are different in static CMOS and novel logics like pass transistor and transmission gates. In transmission gate logic parallel connection was given between nMOS and pMOS networks. Whereas, in pass transistor logic design we use both networks.

Here in our proposal, a 2:4 low power line decoder and 4:16 low power line decoder is designed and simulated. By using this low power 4:16 line decoder a 2-bit comparator was designed and discussed with their power and delay relational aspects. We designed the 2:4 and 4:16 line decoders by using TGL AND, TGL OR and DVL AND, DVL OR gates. Totally we used 4 gates to design 2:4line decoder and 16 gates for 4:16 line decoder. By using this 4:16 line decoder two-bit comparator was designed. Novel topologies and mixed logic design methods are aimed to have low rate of power, area, and delay.

2. Literature Survey

Line decoders are designed using different mixed logics. In this paper, the design of comparator using conventional CMOS and mixed logic approaches were given and a comparative analysis was done with all their parameters taken into consideration in both the designs and simulation results obtained.

D. Balobas a, N. Konofaos [1], in their article they proposed mixed logic designed line decoders to consume less power. They designed 2:4 and 4:16 low power line decoders and also they design 2:4 and 4:16 high performance line decoders to increase the speed with a notable and considerable delay. From this article we learn to design decoders with less power consumption and less delay. These line decoders are used to design comparators in this project with less power, less area and less delay.

A Sharma [2] in his article, he was proposed a less transistor count 4:16 line decoder. They designed 4:16 line decoder using TGL and DVL gates to consume less area. By using this less transistor line decoder, we aimed to design a comparator with an average consumption of power and with a reduced delay. By using this line decoder we can reduce the area of the circuit and also we design area efficient comparator using this 4:16 line decoder.

S. Meena, J.A. Jacob, M. Poornalakshmi and S. Priyanka [3], in their article they suggested the area efficient 2:4 and 4:16 line decoders. They designed 2:4 and 4:16 line decoder using TGL and DVL gates to consume less area. By using this less transistor line decoder, we aimed to design a comparator with an average consumption of power and with a reduced delay [13-15].By using this line decoder we can reduce the area of the

circuit and also we design area efficient comparator using this 2:4 and 4:16 line decoder.

K .Yano, T. Yamanaka, T.Nishida, M. Saitok, K. Shimohigashi and A. Shimizu [4], in their article they proposed the designed circuit using pass transistor and transmission gates, from this both article we designed circuit by using pass transistor and transmission gates to minimize the count, by decreasing area we can decrease power of the circuits.[7-12] By using pass transistors our project consume less area and also decrease the power.

J. C. Lo, [5], proposed a novel area-time efficient static CMOS totally self checking comparator. In this article he designs self checking comparator with less count of transistor. By using this comparator design we design the comparator using line decoder and also area efficient comparator.

G. Sharma, H. Arora, J. chawla and J. Ramizai [6] proposed high performance magnitude comparator by combining both logic designs the low power comparator. In their article they proposed high performance magnitude comparator. They designed to increase speed of the comparator. From this we can know how to design high speed and high performance comparator. By using high performance line decoders we design comparator to increase speed with less area and less delay.

3. Existing Method

3.1 Overview of mixed logic line decoders and comparator circuits

In the era of digital circuits, the information conveyed is in the binary form. Binary form can be represented in 0's and 1's only. Combinations of n bit code was 2^n.Line decoders have 'n' input lines and 2^noutput lines whereas; comparator is in the form of bits example: 2-bit.

A. 2:4 Line decoder and 4:16 line decoder using CMOS logic:

In this 2:4-line decoder we have 2 input line and 4 output lines. In this line decoder FOUR AND gates and 2 NOT gates are used. Instead of AND gate here NOR was used. This circuit AND logic were designed by using NOR because they are universal. For this CMOS circuit we use 20 transistors.

Table I: Truth table of 2:4 Line Decoder

A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

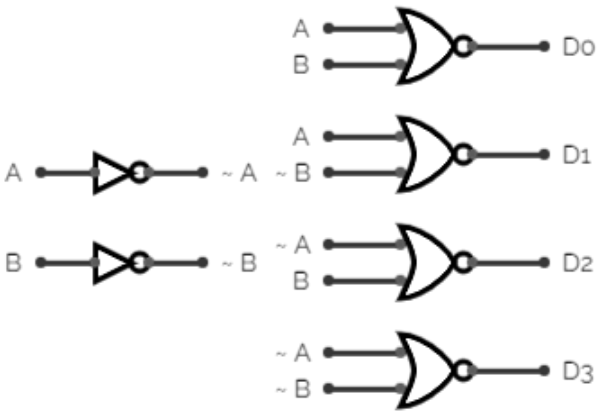

Fig 1: 2:4 Line decoder using NOR gates.

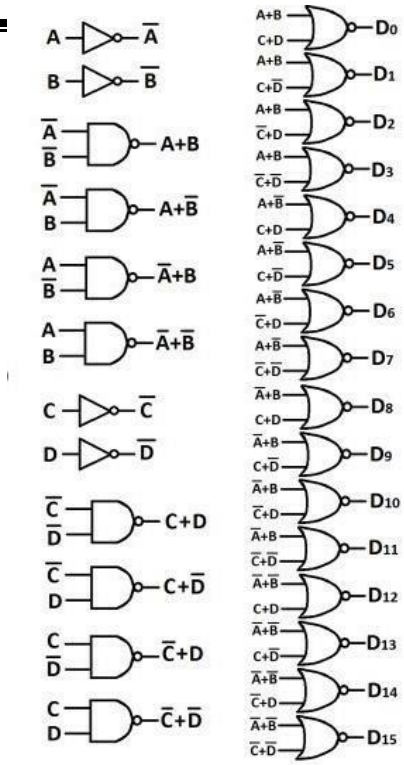

Fig2: 4:16 Line Decoder Using NOR Gates.

B. 2:4 Line decoder and 4:16 line decoder using novel topologies:

In this 2:4- line decoder 14 transistors are used and in 4:16 line decoder 90 transistors are used. Instead of CMOS technology mixed logic of pass transistors and transmission gates are used. By using this mixed logic transistor count decreases it means area decreases, power decreases and delay also will be low.

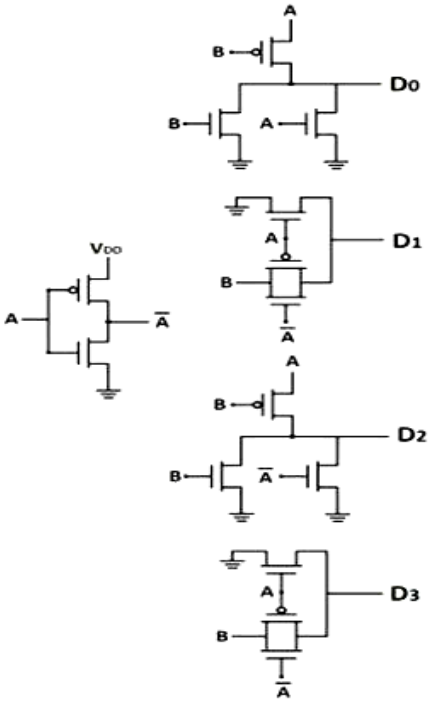

Fig3: Low power2:4-line decoder using TGL and DVL gates.

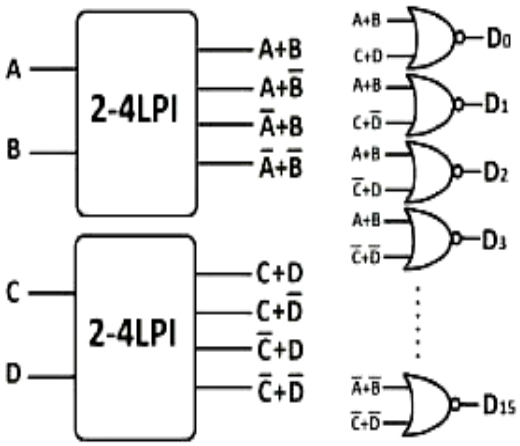

Fig4: Low power 4:16 line decoder using TGL and DVL gates.

4. Proposed method

4.1 Applications of the line decoder

2-bit comparator using 4:16 low power line decoder: 2- bit comparator was designed by using 4:16 line decoder by using pass transistor and transmission gate of mixed logic design method.

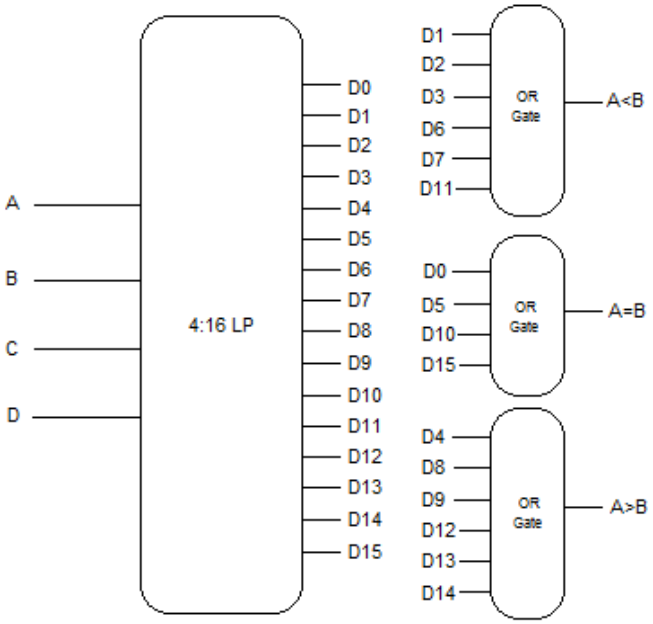

Fig5: 2-bit comparator using low power 4:16 line decoder.

A. 2-bit comparator using 4:16 line decoder:

A 2-bit comparator was designed by using 4:16 line decoder by using Conventional CMOS.

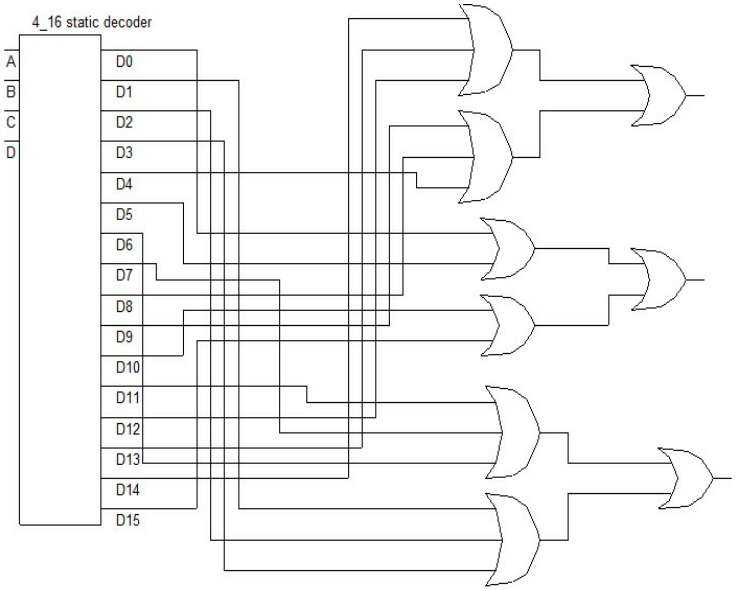

Fig6: 2- bit comparator using CMOS 4:16 line decoder.

In the figure 7, the output of low power 4:16 line decoder is connected to or gates where we use 3 gates to design or gate topology by using pass transistor and transmission gate. Here A, B, C, D are the input lines of line decoder and get D0 to D15 are the output lines of line decoder.4:16 low power line decoder was designed by using 2 2:4-line decoder. That line decoders are designed by using TGL and DVL mixed logic method. By using this method can reduce area, power, and delay.

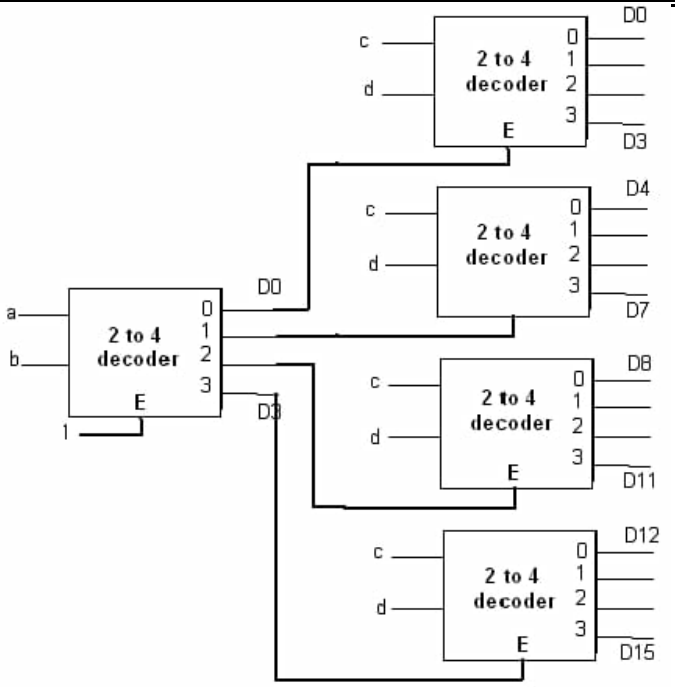

Fig7: A 4:16 low power line decoder.

B. 2-bit comparator using conventional CMOS line decoder

In the figure 8 we may see that 4:16 line decoder was designed by using Static CMOS logic. Here the output lines of 4:16 line decoder connected to inputs of OR gate to perform comparator operation. D1, D2, D3, D6, D7, D11 output lines are connected to OR gate to get output of comparator A< B (out 17). D0, D5, D10, D15 these output lines are connected to second OR gate to get A = B (out 18). D4, D8, D9, D12, D14, D13 these outputs are connected to third OR gate to get output A > B (out 20).

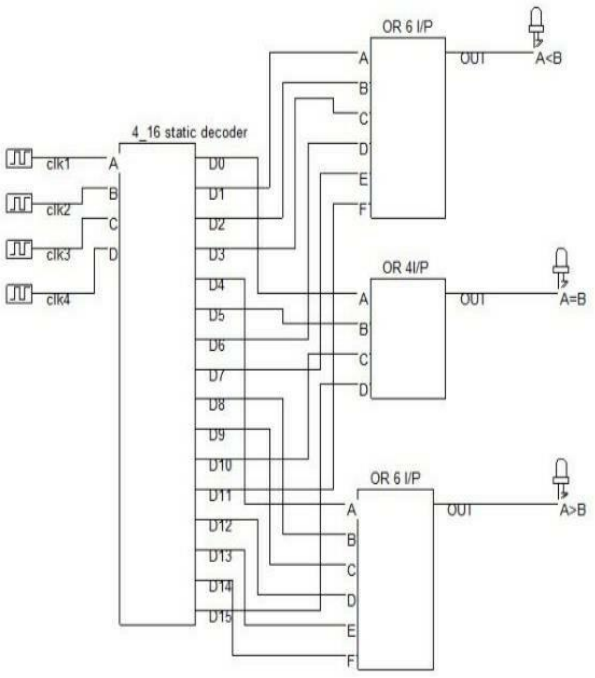

Fig 8: Comparator using Static CMOS 4:16 line decoder

C. 2-bit comparator using mixed logic line decoder

In the figure8 we see that 4:16 line decoder was designed by using mixed logic. Here the output lines of 4:16 line decoder connected to inputs of the OR gate to perform the 2 bit comparator operation.D1,D2,D3,D6,D7,D11 output lines are connected to OR gate to get output of comparator.

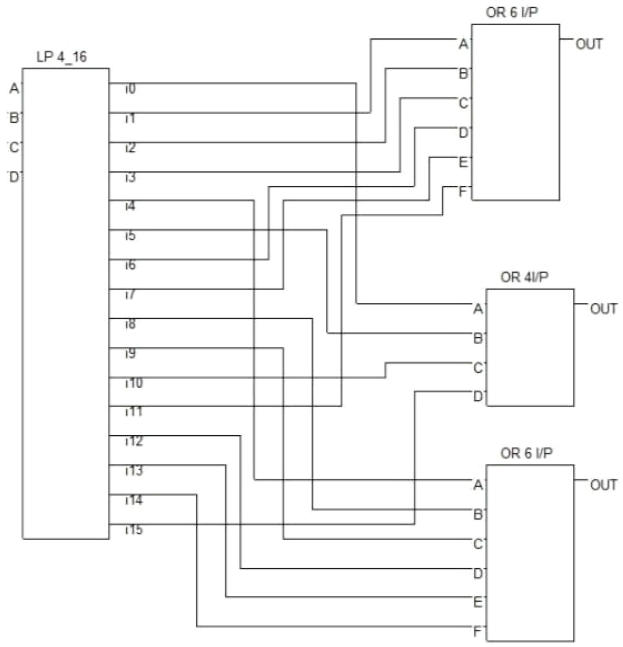

Fig 9: Comparator using 4:16 low power line decoder.

5. Simulation Results

In this simulation we performed the simulations using DSCH and MICROWIND tool to contrast the mixed logic comparator and the traditional CMOS comparator using 4:16 line decoder. All the circuits are implemented by using 7nm technology for area efficient, low power and less delay applications, incorporating the stress effects [4] and high k. We focus mainly on area, low power and delay.

A. Simulation setup:

In this proposal first we designed the circuit using DSCH tool, after that we converted that DSCH file into Verilog file. All the input lines are connected to clock signals and simulated the results in MICROWIND for 100ns.

B. Performance examined:

This compares the total power dissipation. Leakage power consumption has become increase especially at low voltage and sub-micron scaling. It is important as dominant of dynamic one [1]. In our analysis we consider leakage and active currents nothing but static and dynamic. Here we calculated the total power dissipation. Scaling of sub micron continuously at less voltage, consumption of the leakage power was increased to dominate dynamic one [1]. Here the active currents are considered. Both static and dynamic power dissipation are extracted from the below simulation out graph. Also we calculated the consumption of the static power and dynamic power to analyze the result and performance of the designed circuits. We compared the consumption of total power, delay and count of transistors in the before design and novel design also analyzed these three components in the both design approaches.

C. Results and Discussion:

To get the expected result first we designed the circuit using DSCH tool and after that it is converted into Verilog file. This Verilog file now compiled using MICROWIND tool. By selecting a particular node we analyzed the power consumption and delay parameters. The fig 10 and fig 11 representing the circuit simulated results pertaining to the mixed logic circuits with respect to the power dissipation and consumption of power, delay and transistors count. The comparative analysis also given for the parameters like dissipation and consumption of power, raise and fall delays for both CMOS comparator and mixed logic design comparator using line decoders in table 2.

In this simulation we observed the consumption of power reduced from 0.084 mw to 0.082 mW, raise and fall delays from 0.143ns to 0.087 ns when considered the proposed mixed logic design approach for comparator using 4:16 low power line decoder. By comparing these two design approaches, according to simulation results from MICROWIND, we conclude that consumption of power and delay is less in mixed logic design comparator than Conventional CMOS logic comparator. Total power consumption in CMOS conventional comparator is 84.20 µW and for mixed logic is 67.07 µW at a particular selected node. From this result analysis, we proved that mixed logic design comparator consumes less power.

Fig10: Input and output waveform of 2bit comparator using 4:16 CMOS line decoder.

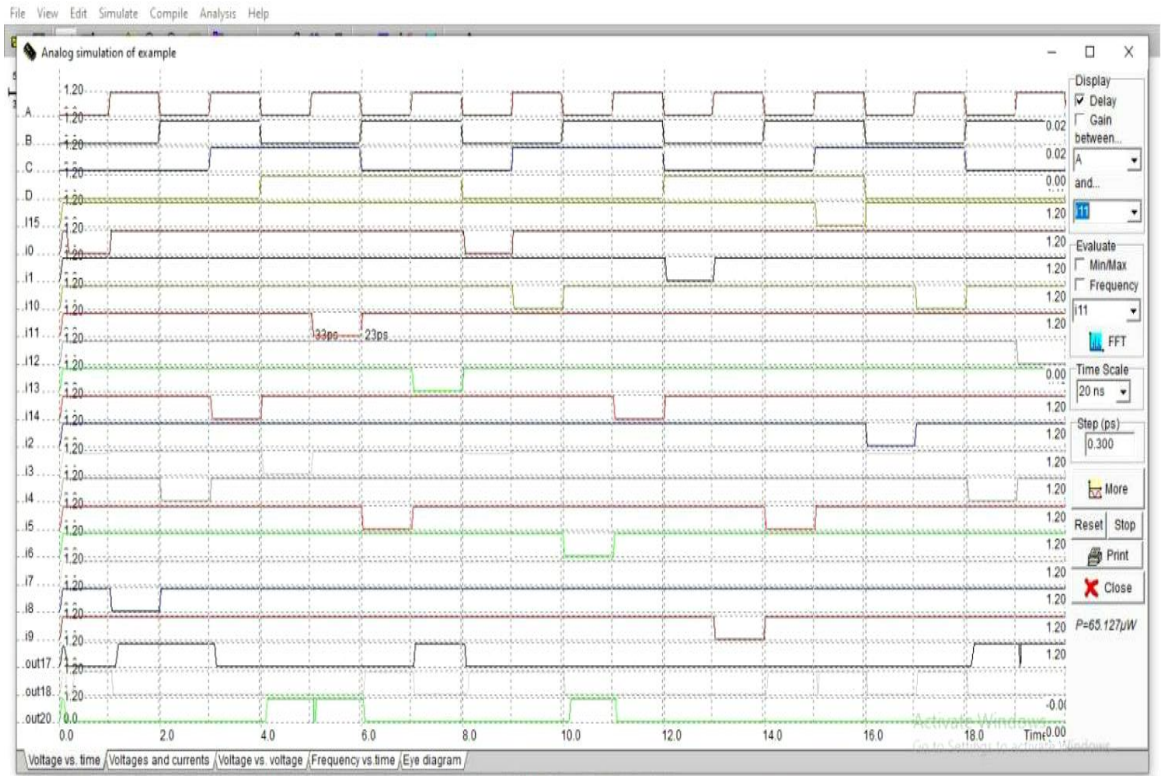

Fig11: Input and output waveform of 2bit comparator using 4:16 low power mixed logic line decoder.

Table II: Comparative analysis of conventional CMOS comparator using 4:16 line decoder with Mixed logic design comparator 4:16 low power line decoder

CMOS comparator using Conventional 4:16 line decoder				**Comparator using mixed logic 4:16 low power line decoder**			
V_{dd}	**Power consumption (mW)**	**Rise delay (ns)**	**Fall delay (ns)**	**V_{dd}**	**Power consumption (mW)**	**Rise delay (ns)**	**Fall delay (ns)**

0.8	0.054	0.394	0.394	0.8	0.046	0.000	0.000
1.0	0.071	0.155	0.154	1.0	0.066	0.181	0.181
1.2	0.084	0.143	0.143	1.2	0.082	0.087	0.087

6. Conclusion

In this paper we introduced mixed logic method to design comparator for better performance metrics like less power consumption and less raise and fall delays. We achieved this by using 4:16 Static CMOS line decoder and 4:16 mixed logic line decoder. Instead of OR and AND gates we used NAND, NOR, NOT gates to decrease the area, power, and delay by decreasing the transistor count. We designed and implemented the line decoder with TGL and DVL and CMOS logic in our proposed design and are compared with conventional CMOS design approach. Finally, we obtained the optimized power circuits and are well implemented on layout level.

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