Design and Implementation of the Turbo Encoder by using Magnitude Comparator in IVS Chip

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ABSTRACT:

This research studies the concept and application of the Turbo_encoder to be an integrated module in the In-Vehicle Device (IVS) embedded module by using the magnitude comparator. To create the Turbo_encoder Module, the complex PLDS are used. The variants of series and parallel Turbo_encoders are discussed. It is shown that proportional to chip size processing time also increased in the Turbo_encoder parallel computing variant system. The magnitude comparator with parallel computing variant system is implemented in this project. The usage of proposed logic resulted in efficient area and power usage. The architecture construction using Verilog HDL and implementation and simulation are executed in the Xilinx-ise tool. To incorporate the built module, Xilinx Vertex Low Power is used. The Turbo_encoder module on a single programmable computer is planned to be part of the IVS chip.

Keywords:

Turbo encoder, IVS chip, FPGA, Xilinx-ise, Simulated, Synthesis.

INTRODUCTION:

Turbo coding is a very effective technique for correcting errors, which in recent years had a huge effect on channel coding. It outperforms all previously developed coding schemes by achieving narrow Shannon limit error corrections using simple part codes and broad interleavers. Typical characteristics of T.E are the iterative encoding process, recursive systematic encoders and the use of interleavers.

Figure 1 displays the modules of the IVS. A Turbo_encoder is used by the IVS as a forward error that corrects (FEC). In data transfers, the Turbo_encoder applies the optical data encoding technique. Turbo coding in digital communication is one of the most common and successful coding techniques for enhancing the bit error rate (BER). On an FPGA unit, the cyclic redundancy search (CRC), the modulator, the demodulator-decoder modules are designed and applied. They were designed to be IVS chip embedded modules.

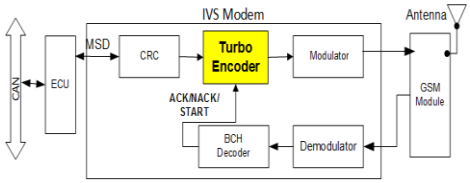

Fig. 1: The complete block diagram of IVS.

LITERATURE SURVEY:

This paper outlines the design and application of the in-vehicle (IVS) emergency contact system (eCall) hardware mechanism in the European Union (EU). On a Field Programmable Gate Array (FPGA) unit, IVS modules are designed and implemented.

The modules are simulated, synthesized and designed as a system-on-chip to be mounted on a reconfigurable device (SoC) For an electronic device from IVS. For checking and verification of the proven materials, the Benchtop test has been performed. The hardware design and the interfaces are discussed. For different frequencies, the IVS signal processing time is analysed. It recommends a set of compatible frequencies and two hardware interfaces. The use of logic has been expanded by more than 72% and loading time has been decreased by less than 59%. The Turbo encoder kit is designed and simulated using Xilinx tools. Xilinx Zynq-7000 is used as an FPGA method to execute the created module. The Turbo encoder module is based on a single programmable computer to be one component of the IVS chip.

Interleaver Design:

A few scientists have since distributed papers on this T.E work, some talking about fundamental interleaver designs, others representing structures that can be utilized to accomplish effective interleaver models. [DIV95a] characterizes a "S-irregular" interleaver, where the components of the interleaver are S = N/2 and N. The technique chooses a number arbitrary incentive inside the Interleaver Size and analyses it to the recently chose numbers of S. In the event that the picked whole number is equivalent to or inside the + S area of one of the past whole numbers chosen, it will be disposed of. The strategy is rehashed until the entirety of the numbers have been picked. [YUA99] determined the "Code Matched Interleaver" or CMI, in which the creators measure the weight scope of codewords with lower weight and use execution investigation to assess the sources of info that contribute fundamentally to the probability of high sign to-commotion proportions of mistake.

The analysts found that the inquiry time was essentially diminished, particularly where high S esteems were normal and the yield was more noteworthy than that of the customary S-irregular interleaver.

TURBO_ENCODER MODULE USING DIGITAL COMPARATOR:

Turbo_encoder is one of the fault error correction methods. The IVS uses a TBmodule with a code rate of 1=3. In the 3GPP standards, the encoder functionalities are detailed. Fig 2 demonstrates the 3GPP Turbo_encoder. The MSD data attached in binary with the CRC parity bits is the turbo encoded input signal. The MSD information block length is 1148 bits. Encoded MSD data in binary is the performance of the module. The output length is 3456 bits by applying the turbo coding Method with 1to3 rate of coding and thrill bits. The thrills structure is accordingly Turbo_encoder.

A parallel concatenated convolution code is used by the Turbo_encoder (PCCC). As is seen in Figure 1, the PCCC is seen with the usage of 2 constituent encoders with 8 states. Zeros are the original status of the registry. The first constituent processes the MSD and applies the convolutional process employed. This takes a bit by bit and provides a bit of parity1 bits. The second constituent applies the

first constituent's equivalent methodology, but after interleaving by a 3GPP-designed interleaver technique, it waits for the MSD bit.

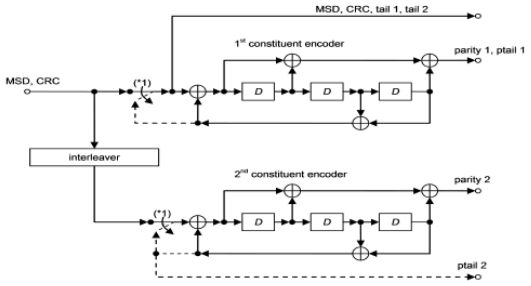

Fig 2: The structural diagram of the working Turbo_encoder.

The length is 1148 bits of the input data included parity1, and parity2. In the tail bits, there are 12 bits. They're powered by input from the change register. The tail bits between the encoded data blocks are added to end points. Figure 2 demonstrates the performance structure of the Turbo_encoder.

MSD+CRC	$tail_1$	$tail_2$	Parity 1	$ptail_1$	Parity 2	$ptail_2$

Fig 3: The Turbo_encoder buffer output

TURBO_ENCODER MODULE BY USING MAGNITUDE COMPARATOR

The technologies are used for the production and implementation of the Turbo-encoder planned module. The Registry Transfer Level (RTL) of the module is integrated into Verilog HDL. For the implementation of the Turbo encoder, several registers are specified. In order to execute the encoding, this study studies two variant solutions.

The serial computation method:

In the serial processing method, reading one bit per single clock cycle is carried out. In a serial method, it reads the MSD input data, constructs the input and output registers and calculates parity1, parity2, and tail pieces. It produces the output bits after completing the encoding. It produces the output bits after completing the encoding. Since the system is standardized and applied, it is noted that it is possible to interfere with the other processes in the module for a long time.

In clock cycles, Ts denotes the running time of the serial variant Turbo-encoder

$$T_s = T_r + T_b + T_{parity1} + T_{tail1} + T_{parity2} + T_{tail2} + T_w \qquad (1)$$

$$T_s = 1148 + 1148 + 1148 + 3 + 1148 + 3 + 3456 = 8054$$

Where Tr is the time taken to read the MSD's 1148 bits, Tb denotes the time it takes to process the output register, Tparit1 is the time it takes to provide parity bits, Ttail is the time it takes to process tail bits, and Tw is the time it takes to get output bits.

The parallel computation method:

The parallel computing method is used in Verilog to create the Turbo-encoder. There are several stages in the serial processing technique that differ when using concurrent processing techniques. In the parallel version of Turbo-encoder computing, there are two functions developed. Almost half of the

running time of the encoding process is extended to all functions. To execute the encoding, the Turbo encoding technique includes the MSD data as a bulk packet. The pseudocode of the applied parallel technique for the Turbo-encoder is seen in the above Figure. With pseudocodes in Verilog, both serial and parallel methods of computation are created. The techniques of serial computing and concurrent computation are denoted by Ts, Tp, one has,

$$T_s = T_r + T_b + T_{parity1} + T_{tail1} + T_{parity2} + T_{tail2} + T_w$$

$$T_s = 1148 + 1148 + 1148 + 3 + 1148 + 3 + 3456 = 8054$$

Tr is the time taken to read the MSD's 1148 bits, Tb denotes the processing time to create the output register, Tparit1 is the time taken to receive parity bits, Ttail is the time to process tail bits, and Tw is the time taken to supply output bits. In parallel processing strategy, the whole process is processed in one clock cycle

$$T_p = 1 + T_w = 1 + 3456 = 3457 \quad (2)$$

Then one has,

$$T_p = 0.42T_s \quad (3)$$

RESUTS

Existed Design Results:

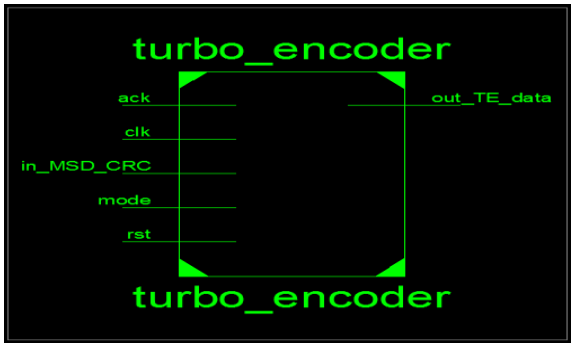

Fig 4: RTL Schematic by using digital comparator

RTL Schematic: RTL schematic is described as register transfer logic that means the logic is transferred to registers it is also known as designer view because of it is looking like what is the intension of designer.

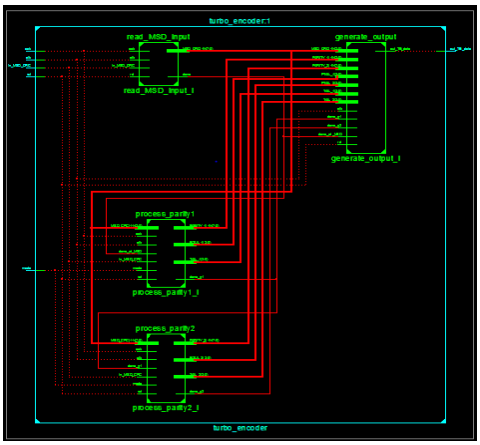

Fig 5 : Internal structure of RTL schematic by digital comparator

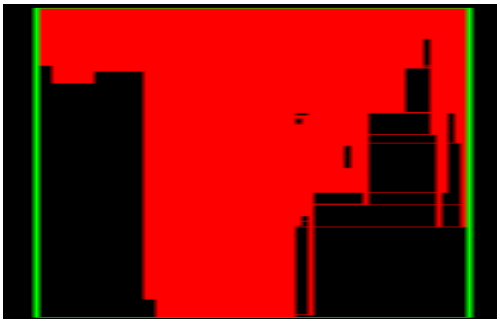

Fig 6: view technology schematic by digital comparator

TECHNOLOGY SCHEMATIC: -

The technology schematic makes the representation of the architecture in the LUT format, where the LUT is consider as the parameter of area that is used in VLSI to estimate the architecture design. the LUT is consider as a square unit the memory allocation of the code is represented in there LUT s in FPGA.

Proposed Design Results:

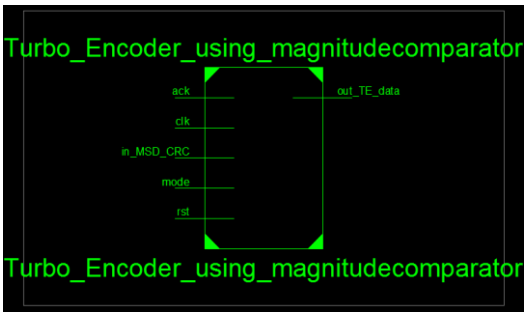

Fig 5: RTL Schematic by using magnitude comparator

RTL Schematic: RTL schematic is described as register transfer logic that means the logic is transferred to registers it is also known as designer view because of it is looking like what is the intension of designer.

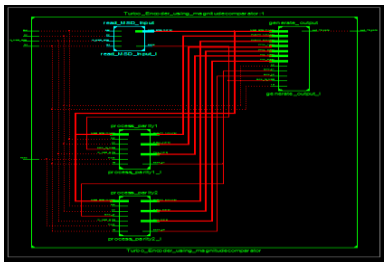

Fig 6: Internal RTL Schematic by using magnitude comparator

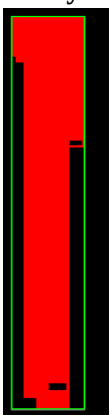

Fig 7: View Technology Schematic by using magnitude comparator

Simulation:

The simulation is the process which is termed as the final verification in respect to its working whereas the schematic is the verification of the connections and blocks. The simulation window is launched as shifting from implementation to the simulation on the home screen of the tool, and the simulation window confines the output in the form of wave forms output. Here it has the flexibility of providing the different radix number systems. In this project serial architecture and parallel methodologies are used. In existed design, digital comparator is used in Turbo_encoder module it utilized 3226 number of Lut's, in Xilinx tool luts are consider as area of design, and it used 54. 113m.Watt power. The magnitude comparator was used Turbo_encoder module was proposed design it consumes 2904 number of lut's 35.124 m.Watt power.

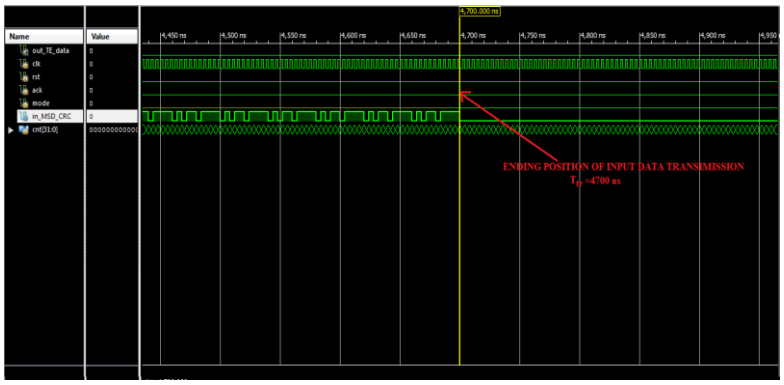

Fig 8: Simulated wave form of serial computation when mode is 0 at time 4700 ns

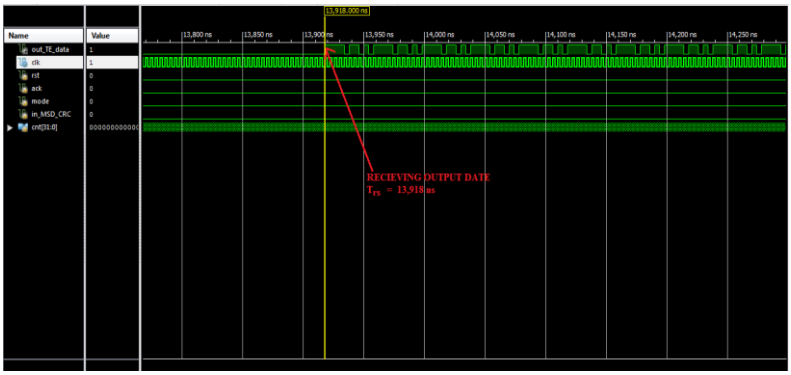

Fig 9: Simulated wave form of serial computation when mode is 0 at time 13918 ns
Required time for serial computation = 13618 – 4700 = 9218 ns

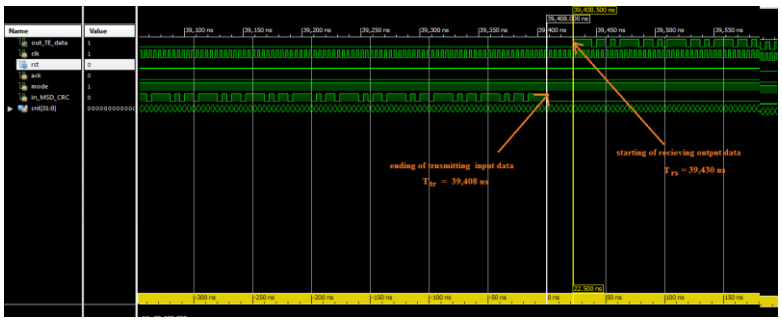

Fig 10: Simulated wave form of paralell computation when mode is 1
Input data transmitting time Ttr = 39408 ns
Output data receiving time Trs = 39430 ns
Required time for parallel computation 39430 – 30408 = 22 ns

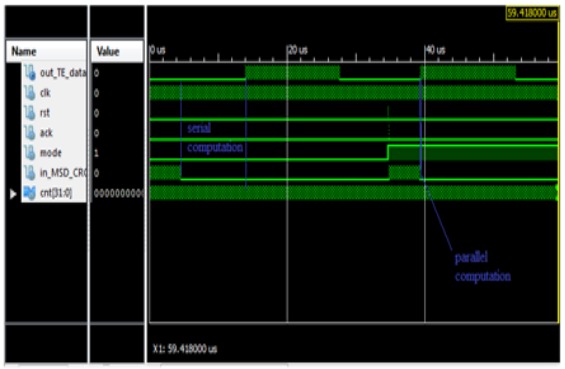

Fig 11: simulated wave form of Turbo_encoder

Table 1: Clock comparison table

Parameter	Serial computation	Parallel computation
Required time to receiving output (ns)	**9218**	**22**

From table 1 the parallel computation method uses less number of clock cycles it will be causes to reduce the power consumption because of 50% of power of the design was utilized by clock pulse only.

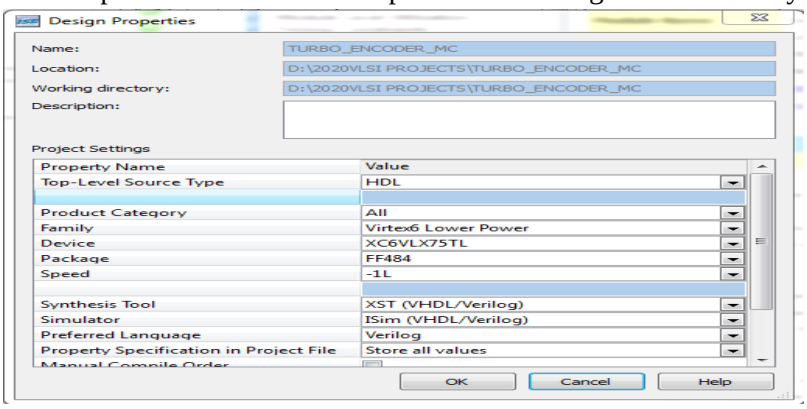

Fig 12: device preferred for simulation

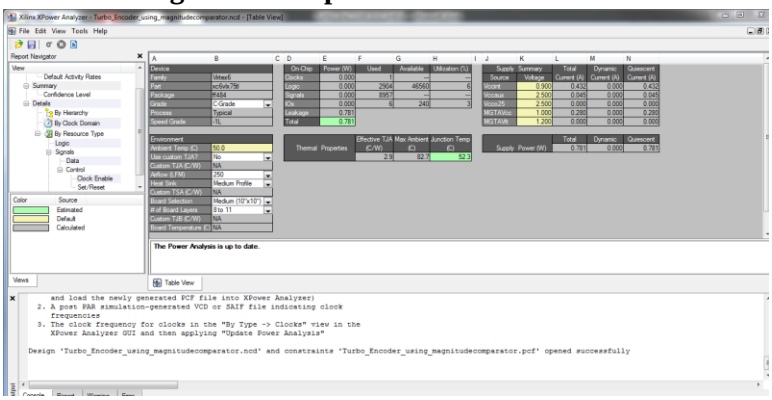

Fig 13: power consumption for vertex low power

Table 2: parameter comparison of existed and proposed designs

Parameter	Turbo_encoder using digital comparator	Turbo_encoder using magnitude comparator

No of LUTs	3226	2904
Power(mWatt)	54.113s	35.124

Advantages & Disadvantages:

Advantages:

The proposed design Turbo_encoder using magnitude comparator utilizes less area and low power consumption. The Turbo_encoders are a class of high-performance forward error correction(FEC) .

Disadvantages:

The Circuit complexity of proposed design Turbo_encoder using magnitude comparator is little bit more compared to existed design Turbo_encoder using digital comparator

Applications:

Turbo_encoders are used in minimum and less error rate communication mediums. Turbo_encoder has also opened up a new way of thinking in the construction of communication algorithms. The Turbo_encoders are used in low latency designs

CONCLUSION AND FUTURESCOPE:

The Turbo_encoder module is designed and implemented to be an integrated module in an IVS modem using a magnitude comparator. In order to build the Turbo_encoder module, FPGA technologies are employed. To build and simulate the module, Xilinx tools and Verilog HDL are employed. For the encoding process, both serial and parallel computing techniques are being studied. The parallel measurement is shown to increase the module's chip size and processing speed. The parallel computing encoding, using just 22 clock pulses, increases the running time and logic utilization by 9218 clock pulses relative to the serial computation strategy. In comparison, as seen in table 2, less area and low power is consumed by the proposed design. The processing time change can be seen in both simulation and chip processing analysis.

The advantages of T.E over current coding systems is that at low signal-to-noise levels it achieves a very low BER, so it can be used in communications. This makes it ideal for wireless applications where low power of communication is required. The efficiency of turbo encodes on the fading channels of Rayleigh and Ricean, however, remains an active subject of study. For code re-usability, the portability of this technology to the Advanced Design System (ADS) would be very useful, and ADS's synthesis technology would also help in faster product growth.

REFERENCES

[1] “eCall data transfer; in-band modem solution; general description,” 3GPP,Tech. Rep. TS26.267.

[2] Eroupean Commission, website: http : //ec:europa:eu/digital –agenda/en/ecall - time - saved - lives - saved.

[3] A. Saleem et at. “Four-Dimensional Trellis Coded Modulation for Flexible Optical Communications,” IEEE Journal of Lightwave Technology., vol. 35, no. 2, pp. 151-158, Nov. 2017.

[4] C. Studer, C. Benkeser, S. Belfanti, and Q. Huang “Design and Implementationof a Parallel Turbo-Decoder ASIC for 3GPP-LTE,” IEEE Journal of Solid-state Circuits., vol. 46, no. 1, pp. 8-17, Jan. 2011.

[5] M. Nader and J. Liu, "Design and implementation of CRC module of eCall in-vehicle system on FPGA," SAE Technical 2015-01-2844, 2015,doi:10.4271/2015-01-2844.
[6] M. Nader and J. Liu. "Developing modulator and demodulator for the EU eCall in-vehicle system in FPGAs" in IEEE, 2016 International Conference on Computing, Networking and Communications (ICNC),Hawaii, USA, Feb. 15-18, 2016, pp. 1-5.
[7] M. Nader and J. Liu. "FPGA Design and Implementation of Demodulator/Decoder Module for the EU eCall In-Vehicle System" in International Conference on Embedded Systems and Applications (ESA'15), Las Vegas,USA, July 27-30, 2015, pp. 3-9.