Design And Implementation of a Digital Secure Code-Shifted Reference UWB Transmitter and Receiver

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ABSTRACT

This paper introduces the concept of overloaded CSRU (Cyclic Shift Register with Accumulator) crossbars as a physical layer solution for Network-on-Chip (NoC) routers. The overloaded CSRU approach enhances channel capacity by utilizing nonorthogonal codes. Two crossbar architectures, namely T-OCI and P-OCI, are proposed to increase the CSRU crossbar capacity by 100% and 2N× 100%, respectively, where N represents the length of the spreading code.

The paper leverages the properties of the Walsh spreading code family, commonly used in conventional CSRU crossbars, to enable a larger number of router ports to share the crossbar without modifying the simple accumulator decoder architecture of the traditional CSRU crossbar. The paper presents procedures for generating nonorthogonal spreading codes and describes the reference and pipelined architectures for each crossbar variant. Both T-OCI and P-OCI crossbars are implemented, and their performance is compared to that of the conventional CSRU crossbar.

The evaluation shows that the T-OCI crossbar achieves a 45% reduction in dynamic power consumption compared to the conventional CSRU crossbar, while the P-OCI crossbar experiences a 133% increase in dynamic power consumption. Furthermore, the T-OCI crossbar utilizes 31% fewer resources, whereas the P-OCI crossbar requires 400% more resources compared to the conventional CSRU crossbar.

To assess the suitability of OCI (Overloaded CSRU with Nonorthogonal Codes) crossbars for NoCs, the paper performs analytical and experimental evaluations on a fully operational OCI-based NoC. A 65-node OCI-based star NoC is implemented and compared to an SDMA-based torus NoC generated by CONNECT. The evaluation results clearly demonstrate the superiority of OCI-based NoCs in terms of area utilization and throughput.

In summary, this paper presents the concept of overloaded CSRU crossbars as a physical layer solution for NoC routers, introduces T-OCI and P-OCI crossbar architectures, and evaluates their performance against the conventional CSRU crossbar. The paper establishes the suitability of OCI-based NoCs through analytical and experimental evaluations, showcasing their advantages in area utilization and throughput.

Keywords: Cyclic Shift Register with Accumulator, NoC router, T-OCI, P-OCI.

1. INTRODUCTION

1.1 Overview

ON-CHIP interchanges significantly affect the general zone, execution, and power utilization of present-day framework on-chips (SoCs). Expanding the correspondence over-head debases the speedup accomplished by parallel figuring as per Amdahl's law [1]. In this manner, creating efficient superior on-chip interconnects has been of central significance for the parallel and elite figuring

advances. Systems on-chips (NoCs) are the most versatile interconnection worldview that is equipped for tending to different application needs and meet distinctive performance prerequisites of substantial remaining tasks at hand [2], including inertness by means of versatile directing [3], throughput by means of enhanced way jumper city [4], control dispersal by streamlining the NoC to focused outstanding tasks at hand [5], and adaptability by run-time design [6]. In NoCs, information is dealt with as parcels, while on-chip handling components (PEs) are considered as system hubs associated by means of switches and switches. NoCs give an adaptable assumption and vast asset overheads [7]. The NoC layering model parts the exchange into four layers: 1) application; transport; 3) system; and 4) physical layers [8]. A crossbar is the fundamental building square of the NoC physical layer. A crossbar switch is a common correspondence medium receiving a numerous entrance procedure to empower physical bundle trade. The fundamental asset sharing systems embraced by existing NoC crossbars are time-division various access (TDMA), where the physical connection is time shared between the interconnected PEs [9], and space-division different access (SDMA), where a committed connection is built up between each match of interconnected PEs [10]. The physical layer of a NoC switch likewise contains buffering and capacity gadgets [7].

1.2 Objective

CSRU is another medium sharing method that uses the code space to empower concurrent medium access. In CSRU channels, each transmit– get (TX-RX) combine is allocated an exceptional bipolar spreading code and information spread from all transmitters are summed in an added substance correspondence channel.

The spreading codes in established CSRU frameworks are symmetrical—cross relationship between symmetrical codes is zero—which empowers the CSRU beneficiary to appropriately disentangle the got entirety through a correlator decoder. Traditional CSRU frameworks depend on Walsh– Hadamard symmetrical codes to empower medium sharing. CSRU has been proposed as an on-chip interconnect sharing method for both transport and NoC interconnect models [11]. Numerous focal points of utilizing CSRU for on-chip interconnects incorporate lessened power utilization, settled correspondence idleness, and decreased framework complex-ity [12]. A CSRU switch has less wiring many-sided quality than a SDMA crossbar and less intervention overhead than a TDMA switch, and in this manner gives a decent trade off both. Be that as it may, essential highlights of the CSRU innovation have been investigated in the on-chip interconnect writing.

Over-burden CSRU is an outstanding medium access method conveyed in remote interchanges where the quantity of clients sharing the correspondence channel is helped by expanding the quantity of usable spreading codes to the detriment of expanding numerous entrance obstruction (MAI) [13]. The over-burden CSRU idea can be connected to on-chip interconnects to build the interconnect limit.

1.3 Problem Statement

In our past works, we connected the over-burden CSRU idea to CSRU-in light of chip transports and exhibited two methodologies, in particular, MAI-based and contrast based over-stacked CSRU interconnects, to expand the transport limit by %25 and half, individually [14], [15] In this paper, we apply the over-burden CSRU idea to NoCs and advance a novel over-burden CSRU interconnect (OCI) crossbar design to build the CSRU switch limit by 100% at minor expense. Crossbar over-burdening depends on misusing extraordinary properties of the utilized symmetrical spreading code set Walsh– Hadamard codes, to include an arrangement of nonorthogonal spread-ing codes that can be exceptionally recognized on the beneficiary side.

2. LITERATURE SURVEY

Hennessy et al. [1] presented the first compact hardware implementation of a digital code-shifted reference (CSR) ultra-wideband (UWB) transceiver. The security of the transmission is based on changing the physical properties of the transmission without the use of higher-level security options. The software models of the designed transceiver are simulated and verified in both floating-point and fixed-point numerical representations. The synthesizable Verilog description of the transceiver architecture is simulated and verified against its fixed-point simulation model. The secure transceiver is implemented on custom-developed field-programmable gate array (FPGA) board.

Tiuraniemi et al. [2] presented a low power, low data rate ultra-wideband (UWB) impulse radio transceiver for location and tracking applications. The UWB receiver is based on a non-coherent, energy collection approach, which makes the receiver highly independent of the shape of the transmitted waveform. The UWB signal is generated by a pulse generator and band-pass filter fixing the signal bandwidth to 1 GHz in the band from 3.1 GHz to 4.1 GHz. The modulation scheme used in this time division multiple access system (TDMA) is Binary Pulse Position Modulation (BPPM). In this paper the system concept, system architecture and RF parts of the VLSI implementation are presented. The transceiver is implemented in a 0.35 μm SiGe process provided by Austria Microsystems.

Siswanto et al. [3] designed the transition metric unit (TMU) using a finite state machine (FSM) and a parallel carry look-ahead adder (CLA) used to design the addition part of the ACSU. After synthesis using Xilinx synthesis technology (XST), the synthesis report shows that the design has a minimum period of 1.888 ns, equivalent to a data rate of 529.661 Mbps fulfilling more than the standard requirements of IEEE P802.15-3a for UWB, which has a data rate range from 55 to 480 Mbps.

Greenwald et al. [4] presented an integrated VLSI system for wireless telemetry of the entire spectrum of neural signals, spikes, local field potentials, electrocorticograms (ECoG) and electroencephalograms (EEG). The system integrated two custom designed VLSI chips, a 16-channel neural interface which can amplify, filter and digitize neural data up to 16 kS/sec and 12 bits and a low power ultra-wideband (UWB) chip which can transmit data at rates up to 14 Mbps. The entire system which includes these VLSI circuits, a digital interface board and a battery, is small, $1.2 \times 1.2 \times 2.6$ in 3 , and lightweight, 33 grams, so it can be chronically mounted on a rat. The system consumed 32.8 mA at 3.3V and can record for 6 hours running from the 200 mAh coin cell battery. Bench-top and in vitro characterization of the system showed comparable performance to the wired recording system.

Farahani et al. [5] proposed a differential ultra-wideband low-noise amplifier using two cascaded flipped-active inductors (CASFAI-LNA). The structure of each CASFAI consists of two transistors (gyrator-capacitor) and a common gate pMOS in its feedback path. The use of the capacitor cross-coupling method increases the transconductance of the circuit, which in addition to improving the gain and the noise figure, reduces the current consumption of the circuit. In addition, the biasing of active inductors from the feedback path reduces the power consumption of the circuit. This circuit is designed and validated in Cadence using a 0.18 μm CMOS process. The post-layout simulation results show that in the whole desired bandwidth (CR frequency range), the input matching is better

than −10 dB, the maximum power gain is higher than 10.6 dB, the minimum noise figure is 2.24 dB, the stability factor is higher than 2.8, and the maximum IIP3 is −2.3 dBm. The proposed LNA consumed 6.12 mW from a 1.8 V DC supply.

Liu et al. [6] presented a fully differential operation broadband CMOS power amplifier (PA) with a power-switchable mode and fast settling time for pulse radar, achieving excellent power consumption, considerable output power, and a -3-dB bandwidth from 3.6 to 6.6 GHz. The on-chip transformer is used for impedance transformation in the output and converting signals from the differential to single ended. Fabricated in a 65-nm standard CMOS process, the operating carrier frequency range of the transmitter covers 3.2-5.8 GHz, and the pulse width can be adjusted from 0.75 to 1.2 ns.

Chang et al. [7] proposed a stable and balanced pseudo resistor applied under a servo feedback loop in a vital-sign receiver of the sensing radar to perform as a high-pass filter (HPF) with an ultralow corner frequency lower than 0.5 Hz for removing undesired clutters of the reflected signals and input dc-offset voltages from innate circuit offsets.

Keshri et al. [8] presented a miniature multiple-input multiple-output antenna that comprised of four elements. The antenna is designed with FR4 substrate whose dimension is 38 mm × 38 mm × 1.6 mm. The antenna consists of four fork-shaped radiators out of two placed on top and two placed on bottom of the substrate. The isolation is improved by placing antenna element orthogonal which gives dual polarization. Further, for more isolation improvement, a decoupling structure has been used between partial slotted ground planes.

2.1 Over-burden CSRU transport topology for MPSoC interconnects

Intra-chip correspondence is a noteworthy bottleneck in present day multiprocessor framework on-chip (MPSoC) outlines. The transport topology is the most well-known on-chip interconnect innovation and transport conflict in one of the significant issues in transport based MPSoC plans. Code division different access (CSRU) has been proposed as a transport sharing system to defeat the transport conflict issue. In CSRU, a predetermined number of symmetrical spreading codes can share the medium because of the Multiple Access Interference (MAI) issue. In remote interchanges, over-burden CSRU has been considered to expand the framework limit by including additional non-symmetrical spreading codes with qualities. We propose a novel CSRU transport design utilizing the over-burden CSRU ideas to expand the most extreme number of centers having the same CSRU transport in MPSoC by 25% at a negligible Improved Overloaded CSRU Interconnect (OCI) Bus Architecture for On-Chip Communication:

Transport topologies and Networks-on-Chip (NoCs) are the fundamental methodologies used to actualize on-chip correspondence. The interconnect texture empowers asset sharing by Time or potentially Space Division Multiple Access (T/SDMA) strategies. CSRU (CSRU) has been proposed to empower asset partaking in on-chip interconnects where every datum bit is spread by a one-of-a-kind symmetrical spreading code of length N. Not at all like T/SDMA, in remote CSRU, the correspondence channel limit can be expanded by defeating the Multiple Access Interference (MAI) issue. Accordingly, we present two over-burden CSRU interconnect (OCI) transport structures, TDMA-OCI (T-OCI) and Parallel-OCI (P- OCI) to expand the traditional CSRU interconnect limit. We execute and approve.

2.2 Over-burden CSRU interconnect for Network-on-Chip (OCNoC)

Systems on Chip (NoCs) have supplanted on-chip transports as the foremost correspondence methodology in vast scale Systems-on-Chips (SoCs). CSRU (CSRU) has been proposed as an

interconnect texture that can accomplish high throughput and settled exchange inertness because of the CSRU transmission simultaneousness. Over-burden CSRU Interconnect (OCI) is a compositional development of the customary CSRU interconnects that can twofold their transfer speed at marginal cost. Utilizing OCI in CSRU-based NoCs has the capability of giving higher transfer speed at low-power and-territory overheads contrasted with other NoC structures. Besides, settled idleness and unsurprising execution accomplished by the inalienable CSRU simultaneousness can lessen the exertion and overhead required to actualize QoS. In this work, we advance the Overloaded CSRU interconnect for Network on Chip

3. PROPSOED METHOD

Overall Structure of CSRU NoC

The basic structure of applying CSRU technique to NoC with a star topology is shown in Fig. 1. In this figure, a PE executes tasks of the application and network interface (NI) divides data flows from PE into packets and reconstructs data flows by using packets from NoC. In the sender, packet flits from NI are transformed to a sequential bit stream via a parallel-to-serial (P2S) module. This bit stream is encoded with an orthogonal code in the Encoding module (E in Fig. 1). The coded data from different encoding modules are added together in the Addition module (A in Fig. 1). Then, the sums of data chips are transmitted to receivers. In the receiver, Decoding modules (D in Fig. 1) reconstruct original data bits from the sums of data chips. Then these sequential bit streams are transformed to packet flits by serial-to-parallel (S2P) modules. Finally, these packet flits are transferred to NI. In the CSRU NoC, network scheduler receives the transmitting requests from senders and assigns proper spreading codes to the senders and requested receivers. Note that all-zero codeword is assigned to nodes having no data to transmit/ receive. Moreover, when there are multiple senders requesting the same receiver, the scheduler will apply an arbitration scheme, for example, round-robin. The chip counters calculate how many orthogonal chips are used in one encoding/decoding operation. Each node needs two chip counters, one for the sender and the other for the receiver. Note that packet flits from NI can also be transformed to multiple bit streams in the P2S module to make tradeoffs between power/area cost and packet transfer latency, and the scheduler should provide a bit-synchronous scheme to maintain the orthogonality of the transmitted channels, as discussed in [8]. In this brief, we focus on the design and comparison of WB- and SB-based CSRU encoding/decoding method, which corresponds to E, A, and D modules.

CSRU Encoder

Two different encoding methods, WB encoder and SB encoder, are compared in Fig. 2. Fig. 2(a) shows the WB encoder architecture. An original data bit is first encoded with a Walsh code by taking an XOR operation. Then, these encoded data are added up to a multibit sum signal by taking arithmetical additions. Each sender needs an XOR gate, and multiple wires are used to express the sum signal if we have two or more senders. Moreover, the number of wires increases as the number of senders increases. Fig. 2(b) shows our SB encoding scheme. An original data bit from a sender is fed into an AND gate in a chip-by-chip manner, and it will be spread to n-chip encoded data with an orthogonal code of a standard basis. The relationship between a bit and a chip is shown in Fig. 3. Then, the encoded data from different senders are mixed together through an XOR operation, and a binary sum signal is generated. Therefore, the output signal is always a sequence of binary signal transferred to destination using one single wire. The progressions of both the encoding schemes are depicted in Fig. 3. Fig. 3(a) and (b) illustrates the WB encoding process with four-chip Walsh codes and the SB encoding process with four-chip standard orthogonal codes, respectively

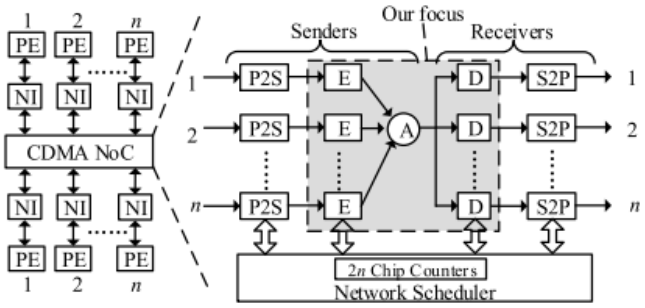

Fig. 1: CSRU-NoC.

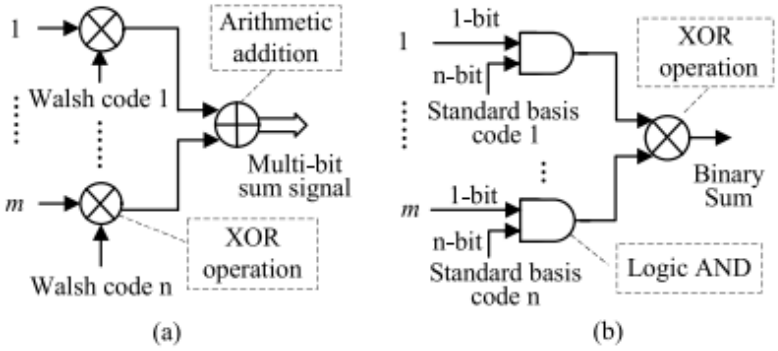

Fig. 2: Block diagram of encoding scheme (a) WB encoder (b) SB encoder.

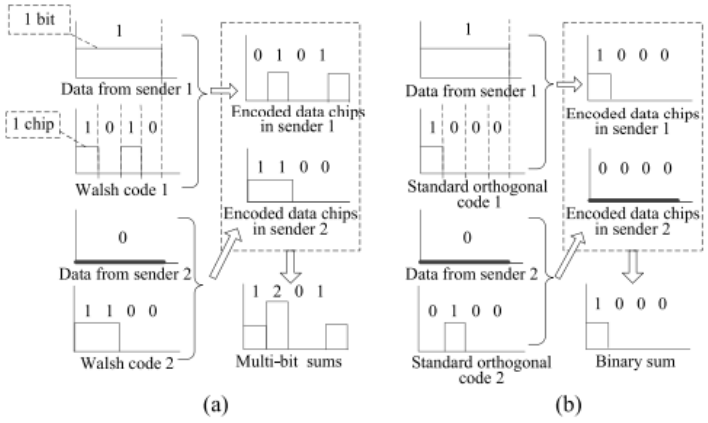

Fig. 3: Data encoding example (a) WB encoding (b) SB encoding.

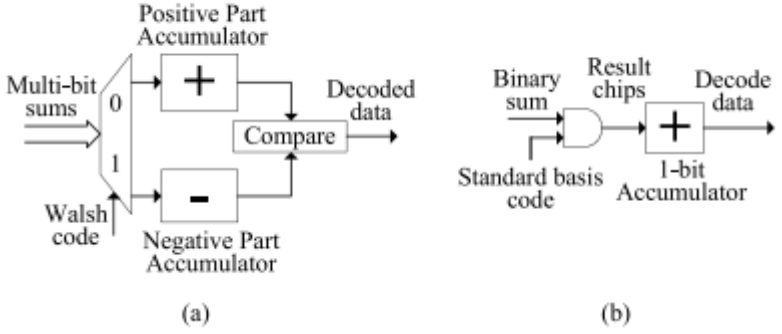

Fig. 4: Block diagram of encoding scheme (a) WB encoder (b) Sb encoder.

CSRU Decoder

The WB decoding scheme is presented in Fig. 4(a). According to the chip value of Walsh code, the received multibit sums are accumulated into positive part (if the chip value is 0) or negative part (if the chip value is 1). Therefore, the two accumulators in the WB decoder separately contain a multibit adder to accumulate the coming chips and a group of registers to hold the accumulated value. Through the comparison module after the two accumulators, the original data is reconstructed. If the value of positive part is large, the original data is 1. Otherwise, the original data is 0. The SB decoding scheme is shown in Fig. 4(b). When the binary sum signal arrives at receivers, an AND operation is taken between the binary sum and the corresponding orthogonal code in chip-bychip manner. Then, the result chips are sent to an accumulator. After m-chips are accumulated (m is the length of the orthogonal code), the output value of the accumulator will be the corresponding original data. Note that there is always only one chip equal to 1 and all othechips are equal to 0 for an orthogonal code in standard basis. Hence, the maximal accumulated value in the SB accumulator is 1 and it can be stored in a 1-bit register. Therefore, in the SB decoding module, only one AND gate and an accumulator with one 1-bit register are used, resulting in less logical resources. An example of the decoding process is illustrated in Fig. 5. In Fig. 5(a), at the WB decoder of receiver 1, the accumulated value 3 in the positive part is larger than the accumulated value 1 in the negative part. By the WB decoding scheme, the decoded data is 1, which is equal to the source data bit from sender 1. In Fig. 5(b), at the SB decoder of receiver 1, the output value of the accumulator is 1, which is also equal to the source data bit from sender 1. Note that the decoding results in receiver 2 are also correct, but are not shown in the figure. Hence, both methods can reconstruct the original data bit from the sum signal by using their respective spreading codes.

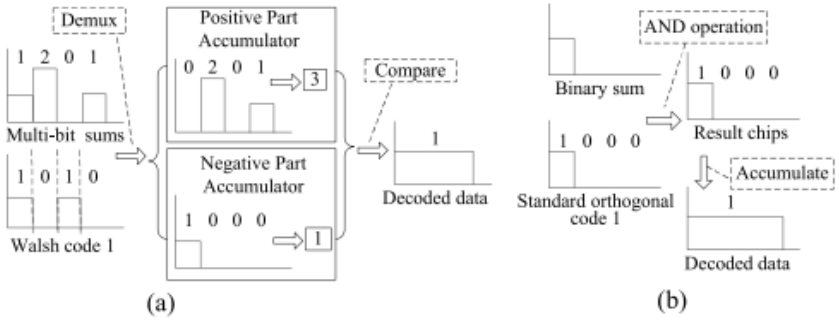

Fig. 5: Data decoding example (a) WB decoding at receiver 1 (b) Sb decoding at receiver 1.

4. SIMULATION RESULTS

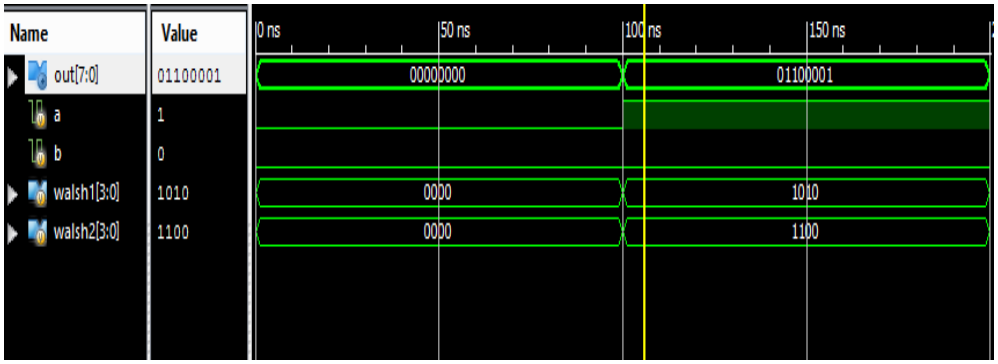

Fig. 6: WB encoder.

The encoded data from two senders are mixed through xor operation, and a binary sum signal is generated. Therefore, the output signal is always a sequence of binary signal transferred to destination using one single wire. The progression of both the encoding schemes are depicted. In WB decoding scheme the chip value of Walsh code, the received multi bit sums are accumulated positive part or negative part by using comparator we have to compare positive and negative parts, if positive is greater than negative then the original data is 1, otherwise the original data is 0.

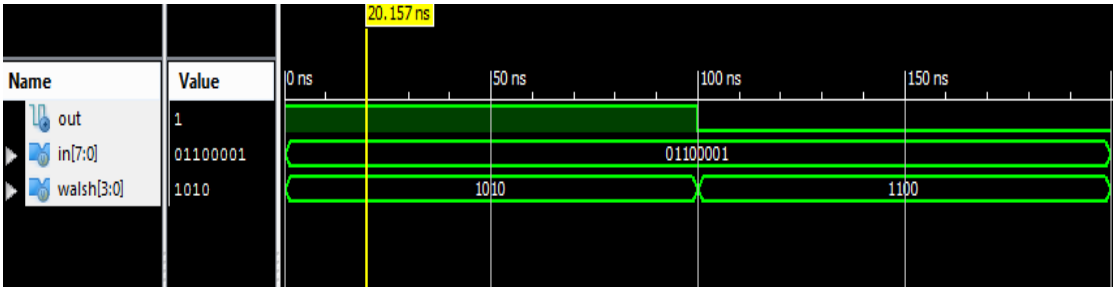

Fig. 7: WB decoder.

SB encoding scheme original data bit from a sender is fed into an AND gate in chip-by-chip manner and encoded data from different senders are mixed together by an xor operation and a binary sum signal is generated. In sb decoding scheme the binary sum signal arrives at recevers,an AND operation is taken between binary sum and corresponding sum then the result is send to an accumulator the output of the accumulator will be the corresponding original data.

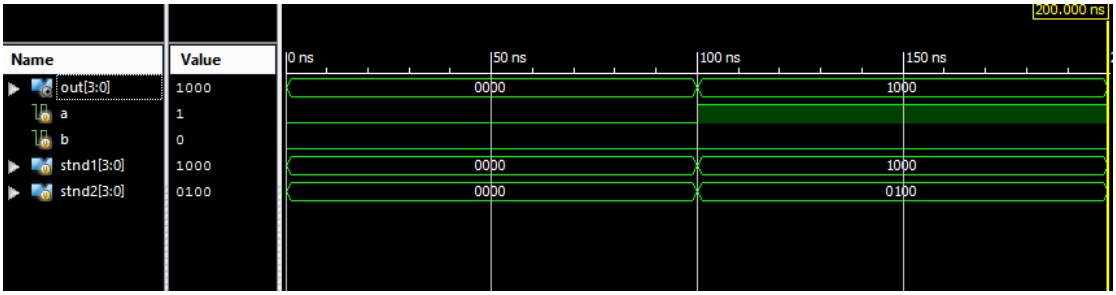

Fig. 8: SB encoder.

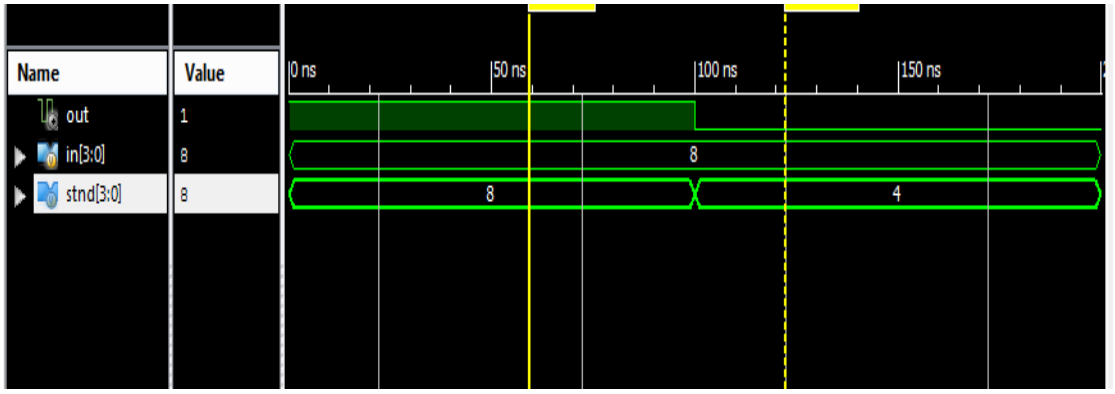

Fig. 9: SB decoder.

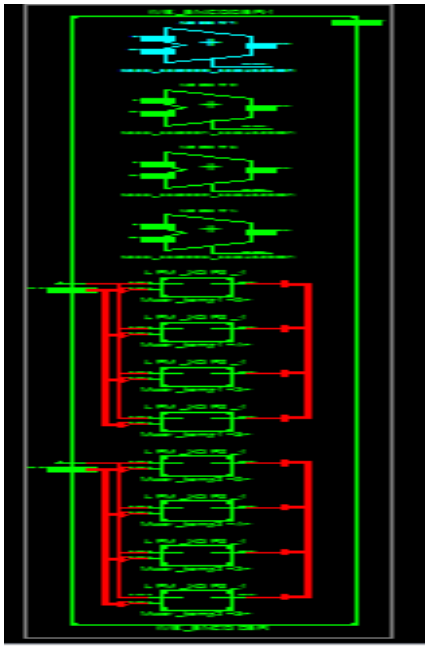

Fig. 10: Rtlschrmatic**.**

Design summary

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	4	5888	0%
Number of 4 input LUTs	8	11776	0%
Number of bonded IOBs	18	372	4%

```
Timing constraint: Default path analysis
  Total number of paths / destination ports: 32 / 8
--------------------------------------------------------------------------------
Delay:               7.337ns (Levels of Logic = 3)
  Source:            b (PAD)
  Destination:       out<6> (PAD)

  Data Path: b to out<6>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             8   0.849   0.900  b_IBUF (b_IBUF)
     LUT4:I0->O            1   0.648   0.420  out<6>1 (out_6_OBUF)
     OBUF:I->O                 4.520          out_6_OBUF (out<6>)
    ----------------------------------------
    Total                      7.337ns (6.017ns logic, 1.320ns route)
                               (82.0% logic, 18.0% route)
```

5. CONCLUSION

In this paper, we introduced the concept of overloaded CSRU crossbars as the physical layer enabler of NoC routers. In overloaded CSRU, the communication channel is overloaded with nonorthogonal codes to increase the chan-nel capacity. Two crossbar architectures that leverage the overloaded CSRU concept, namely, T-OCI and P-OCI, are advanced to increase the CSRU crossbar capacity by

100% and 2*N*× 100%, respectively, where *N* is the spreading code length. We exploited featured properties of the Walsh spread-ing code family employed in the classical CSRU crossbar to increase the number of router ports sharing the crossbar without altering the simple accumulator decoder architecture of the conventional CSRU crossbar. Generation procedures of nonorthogonal spreading codes are presented along with the reference and pipelined architectures for each crossbar variant. The T-/P-OCI crossbars were implemented. The performance of the OCI crossbars is compared with that of the conventional CSRU crossbar. The dynamic power is reduced by 45% for the T-OCI crossbar but increased by 133% for the P-OCI crossbar. The T-OCI crossbar utilizes 31% fewer resources, while the P-OCI crossbar uses 400% more resources compared with the conventional CSRU crossbar. The OCI crossbar suitability for NoCs has been established by analytically and experimentally evaluating a fully working OCI-based NoC. A 65-node OCI-based star NoC was realized and compared with an SDMA-based torus NoC generated by CONNECT. The evaluation results demonstrate the superiority of the OCI-based NoCs in terms of area and throughput.

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