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Research Article

Performance analyzes of RNS-FIR filter using prefix accumulation based DA arithmetic

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Abstract*: This study describes the design of high speed FIR filter design with low complexity using various types of adders and multiplication methods. This work also explores the significance of prefix addition in path delay reduction and it's accelerating performance in various DSP applications. The FIR filters consist of two core functional units such as adder and multiplier. In many existing FIR filter designs the system performances are accelerated using various multiplication methodologies and some optimization techniques. This paper briefly investigates the necessities of the parallel prefix adder in path delay reductions and the influence of multiplier less FIR design in overall system performance. And conclude the performance metrics and trade off measures between complexity and path delay optimization level of various types of Prefix adders and multipliers. This work focuses on both high speed accumulation and multiplication units for high performance FIR filter design and its performance is compared with the existing FIR filter design in terms of delay and hardware utilization rate.

Keywords: Prefix accumulation, RNS system, FIR design, FPGA, Low Powe etc.

I. INTRODUCTION

Most modern digital systems include signal filtering over a wide range of applications which demand both throughout rate and energy efficiency with optimal arithmetic modeling. In general inner product computation and successive accumulation unit are used as core processing elements in wide range of DSP applications such as correlation [1], FIR filtering and convolution [2] etc. . For product computation Distributed Arithmetic (DA) is a predominant technique for calculating for performing multiplier less computation for low complexity [3]. For delay optimized addition, , the prefix topology allows the parallel computation and carry propagation less accumulation where number of stages can be alerted according to the data length of the data involved.

Residue Number System (RNS) is considered as potential alternative to accomplish both area efficiency and high speed FIR filter due to its parallelism and small data bit-length. In RNS system dynamic range of input operands is regulated based on appropriate residue generation using optimal moduli sets. However, still there are several issues need to be solved when implementing the RNS system in FIR filter to outperform DA based inner product generation and prefix based data accumulation in practice. Furthermore, the implementation of the reverse co version also rather restricts the influence of RNS system in high performance FIR filter. The potential consideration in using RNS in FIR filter design is likely depends on parametric requirements adopted in real time applications [4-5].

This survey work is organized as follows. Section II provides the detailed analyzes of prefix techniques and various DA methods used for FIR filter design for product calculation, and potential metrics of RNS and its advantageous in FIR filter implementation. Section III summarize the parametric comparative analyzes of various FPGA implementations of RNS FIR system. Section IV concludes the details

II. FINITE ARITHMETICS FOR HIGH PERFORMANCE FIR FILTER DESIGN

A. FIR filter design

In general for finite impulse response driven filtering operation convolution is performed as a weighted finite term sum, of past, present, and perhaps future samples of the filter input. The output response is given by

$$y[n]=\sum_{k=0}^{N-1} b_k \cdot x[n-k]$$

(-)

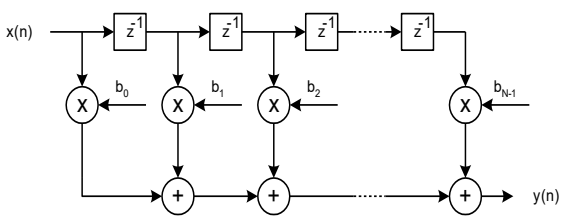

Fig. 1. Generic FIR architecture

. An FIR filter of length N is formulated by N+1 filter coefficients requires N+1 multiplication and N accumulation unit. The direct form FIR structures are a unique methodology used for deriving the FIR coefficients and filter taps incorporated for transfer function. But it has limitations of increased amount of computation needed to process the input signal and affects overall system performance in terms of attainable speed. This will limit the feasibility of using FIR for wide range of real time applications.

B. DA arithmetic

In DA based arithmetic multiplication through multiplier less partial product generation exhibits a better quality metrics as compared to all other high performance multiplier models [6]. It is incorporated as follows: During PP computation all the inputs are computed identically and zeros irrelevant to end products are coordinated with other. Several research works proved that residue number system (RNS) can give significant hardware complexity reduction as compare to all other optimization models.

Table- I: Summary of research gaps in previous prefix topology

Title	**Author name**	**Method used**	**Merits**	**Limitations**
Comparative Analysis of Parallel Prefix Adders, 2013 [8]	Talsania, Megha, and Eugene John	Parallel prefix adders	Analyzed the performance of six different parallel prefix adders implemented using four different TSMC technology nodes.	Both size and complexity increased with bit width size and Lacks with integrity.
Area Efficient Hybrid Parallel Prefix Adders, 2014 [9]	Poornima et al.	Hybrid Parallel Prefix Adders	Ladner-Fischer approach for even-indexed and KoggeStone structure for odd-indexed bits.	The complexity of the generate term is reduced only in the first level of prefix tree.
Wallace tree multiplier using compressors and parellel prefix adders, 2016 [10]	Masumdar et al.	Wallace tree and PPA	Wallace tree multiplier with Multiple compressors in parallel increase the throughput	Only 41% reduction in the delay as compared to the conventional ripple carry adder
Use of Parallel Prefix Adder Topologies into Approximate Adder Circuits, 2017 [11]	Macedo et al.	Approximated PPA	, Error Tolerant well-known approximation is used for PPA Addition	Improved clock frequency up to 2.22 times with a maximum energy consumption overhead of 7.4%.
Performance Analysis Of Parallel Prefix Adder For Data path, 2018 [12]	Shilpa, et al.	Prefix topology	Due to high degree of parallelism Ladner-Fischer Adder configuration gives best trade off between area and delay.	Latency will occur since PPA possesses maximal depth

In general, DA based PP generation and accumulation for FIR filer design which has following advantages.

1) Multiplier less partial product computation will offer considerable complexity reduction over wide range of operand set.

2) It can be used for higher order FIR design to solve trade off constrains related to conventional MAC system.

3) Path optimized carry propagation at the final stage of PP accumulation can improve speed of MAC operation with appropriate data accessibility. The literature survey has covered the work on both prefix accumulation and various DA arithmetic models as shown in Table I and table II. The issues

and challenges have been identified and are overcoming the limitations using RNS system which is described in the next chapter.

C. Parallel prefix accumulation

In prefix computation carry generation and all other preprocessing stages follows the same techniques as like a Carry Look Ahead Adder [7]. However the generation of the carriers and propagation, prefix topology designed in many different ways based on trade off measures and system requirements. In general tree based structure is used to formulate prefix tree to increase the speed of arithmetic operation. Parallel prefix adders come with least critical path due to optimal carry propagation and this tree based hierarchical structure attains high performance and widely used accumulative model in many digital industries. Several different parallel prefix adders are available. Brent-Kung and Kogge-Stone adders are very popular.

D. Speculative shift/add MAC

Here multiplier less shift/add scheme is used for inner product generation for MAC process. Each tap holds single bit which is driven by shifting controller. All incoming bits are detected for binary 1's and appropriate shifting operations are coordinated. Speculative prefix accumulations are stated here as core inner processing elements for each MAC end results and overall system performance is driven by PPA accumulation. During partial product generation adder units sequentially instantiated with appropriate MSB bit extension to accommodate dynamic range extension due to multiplication operation.

Table- II: Performance analyze of various distributed arithmetic models for FIR filter implementation

Title	Author name	Method used	Merits	Limitations
Optimized Canonic Signed Digit for FIR filter design, 2015 [13]	Jia, Rui, et al.	Canonic Signed Digit	Here heuristic approach based on Particle Swarm Optimization is used to narrow down binary weightages.	It has restrictions towards dynamic range of FIR coefficient values.
Multiplier-Less Non-uniform CSE Technique, 2017 [14]	Sharma et al.	Common sub-expression elimination	Artificial bee colony algorithm is used for optimization.	Complex pre-computation is required and its level of computational burden increased with FIR length
Area-efficient bit-level Radix-2^r is used for low complexity, 2017 [15]	Liacha, Ahmed et al.	Bit serial DA	Multiple constant multiplication (MCM) algorithm is used to optimize cumulative accumulation	Excessive bit- serial path overhead leads worst case critical path.
Use of Wallace tree Topologies into Approximate DA units, 2018 [16]	Jiang, Honglan, et al.	Approximated Distributed Arithmetic	Bit-level pruning during accumulation of partial products	Though no multiplication is explicitly used the sum operation significantly limit the optimization rate
LUT based Area Efficient Pipelined DA for Adaptive FIR Filter, 2019 [17]	Jyothi, et al.	Decomposed LUT model	Due to pipelined lookup table data collection path delay is reduced.	Latency will occur due to inner stage pipelining among tap computations

III. RNS FIR FILTER DESIGN

At present, RNS systems are widely investigated in many DSP applications for achieving area efficiency, high throughput rate etc. Nonetheless, to design and MAC unit that meets design requirements of FIR filter and to narrow down penalty gap that exist attainable performance measures over actual rate demands. This Distributed arithmetic involves no carry propagation in accumulation and pre-computed LUT blocks to attain maximum operating speed and least possible hardware complexity overhead in FIR filter design. In [14] integrates the RNS accumulator with radix-4 high performance booth multiplier to accomplish flexibility and low complexity in FIR filter design. This method also includes pre-loaded product block to minimize the computational cost and delay during partial product generation for each FIR taps.

A. Advantages of RNS system

High Performance: The absence of carry propagation during successive arithmetic blocks results in high speed computation.

Energy efficiency: Higher order input operands are decomposed into smaller arithmetic units while realizing the RNS system minimize the digital transition activities during MAC operations for each taps. This transition reduction limits the dynamic power consumption, since the dynamic power is directly proportional to 1-0 or 0-1switching activities.

Hardware Complexity reduction: During RNS computation moduli conversion encodes the input operands into small values caused residues, the resource requirements to carry out any sort of arithmetic operation on these residues are optimally far less as compare to direct implication. This will regulate the arithmetic accumulation and optimize the overall design.

The accumulation of various moduli sets and its size makes the RNS system effective in FPGA hardware implementation. In this section, some of the few important experimental measures are observed in various FPGA based RNS FIR design such as power dissipation, network data rate, and RNS model used for residue computations etc. These are presented in table III.

Table- III: Performance metrics comparison of RNS FIR filter design systems

Methods	**Author name**	**RNS Model used**	**Input /Coefficient size**	**FPGA device used**	**speed (MHz)**	**Power dissipation**
Distributed arithmetic (DA) based RNS FIR design, 2004 [18]	Wang et al.	Five moduli sets,	14-bit unsigned	Xilinx Virtex 300	55MHz	826mW
6-input Look-Up Table based RNS FIR design, 2012 [19]	Pontarelli et al.	Four moduli sets,	8-bit unsigned	Xilinx XC2064	545 MHz	-
Accumulator based radix-4 booth for RNS filter design , 2014 [20]	Pari et al.	Three moduli set	24-bit signed	ALTERA cyclone II	715.31MHz	119.36mW
Booth radix-8 encoded RNS FIR design, 2016 [21]	Goel, et al.	Three moduli set	32-bit signed	Xilinx Spartan 3E	350MHz	-
Core Functional decimal equivalent binary conversion RNS FIR design, 2017 [22]	Prakash et al.	Five moduli set	32-bit unsigned	Xilinx Spartan 3E	230MHz	175mW
Double Base Ternary Number System (DBTNS) multiplier with carry free arithmetic operations for RNS FIR design, 2018 [23]	Ghosh et al..	Three moduli set	32-bit unsigned	Xilinx Virtex 7 XC7VX1140T	309.377MHz	
Device dependent efficient Boolean map network is used for RNS FIR design,2018 [24]	Khurshid., et al.	Three moduli set	16-bit unsigned	Xilinx XC5VLX50-2FF324	525.88MHz	772.41mW

IV. CONCLUSION

This paper presents an extensive survey on various prefix topology and DA techniques and its metrics over modeling high performance FIR filter design etc. Many efficient RNS techniques are also analyzed over various FPGA implementations etc. Some research issues are highlighted in RNS system incorporation for DSP applications and penalty gaps need to be narrow down to mitigate the trade off problems that exists with various dynamics of digital FIR filer design in real time applications.

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